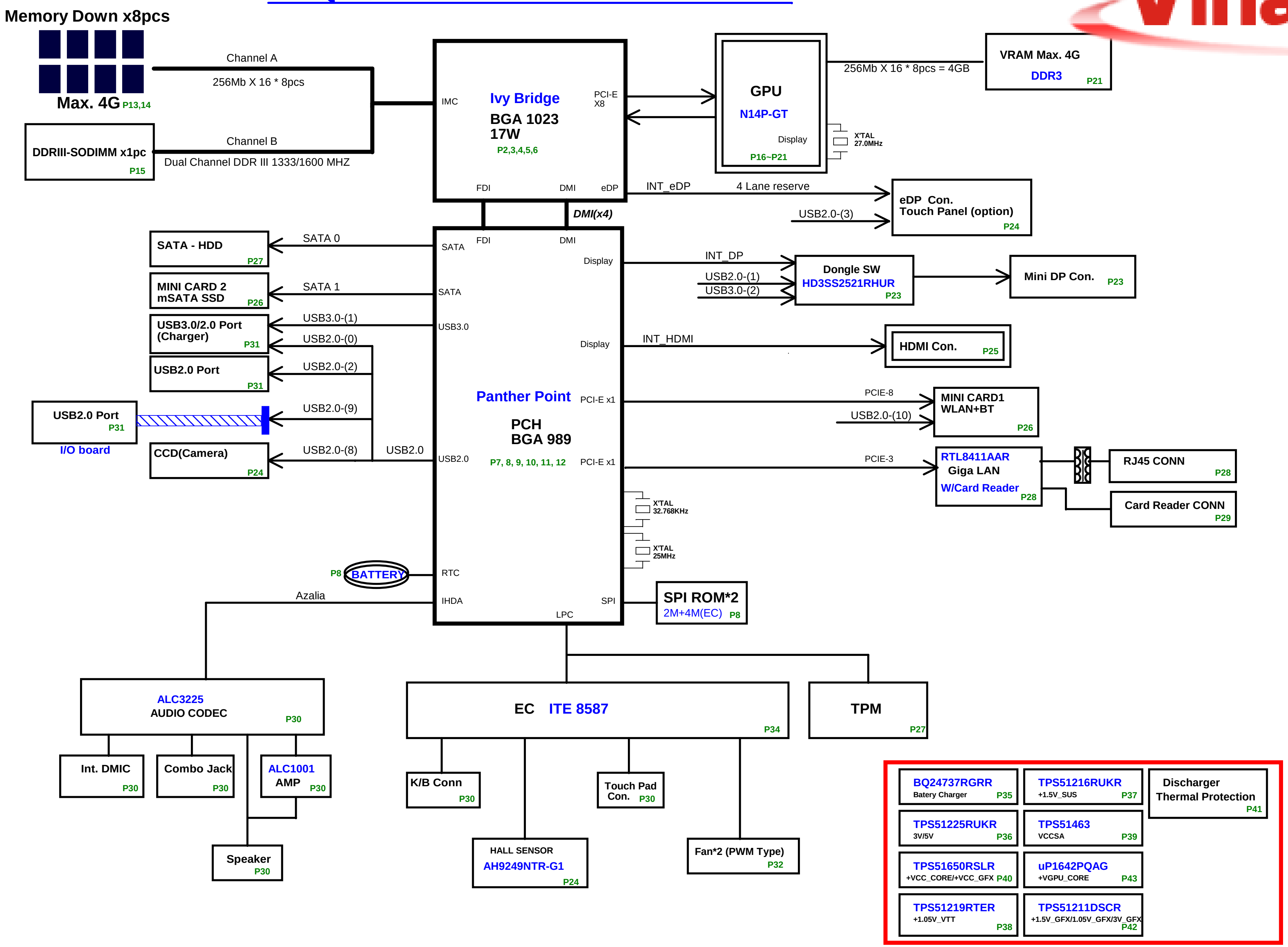
ZQK ULV SYSTEM BLOCK DIAGRAM



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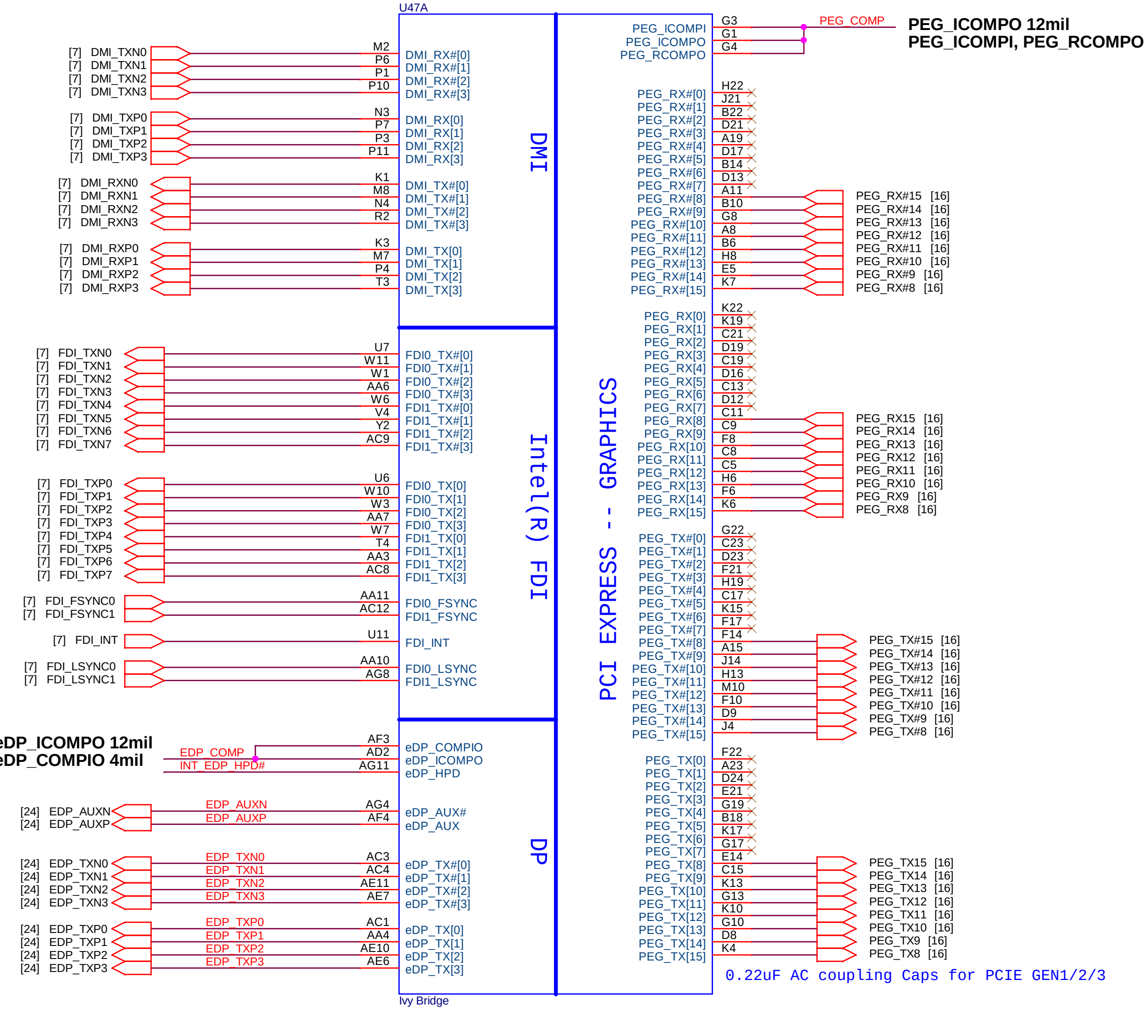
Ivy Bridge Processor (DMI,PEG,FDI) (CPU)

PEG_ICOMPI and RCOMPO signals
should be shorted and routed with
- max length = 500 mils
- typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with
- max length = 500 mils
- typical impedance = 14.5 mohms

PEG_ICOMPO 12mil
PEG_ICOMPI, PEG_RCOMPO 4mil,



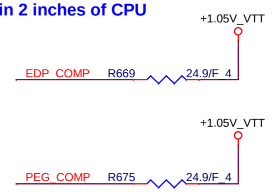
0.22uF AC coupling Caps for PCIE GEN1/2/3

DP_COMPIO and ICOMPO signals
should be shorted near balls and routed with
- typical impedance < 25 mohms

DG 1.0 :
The recommended AC cap value is changed to 220nF for compatibility with
PCIe Gen3 on future platforms.
For Gen2 only designs, it is acceptable to continue to use the 100nF capacitor.

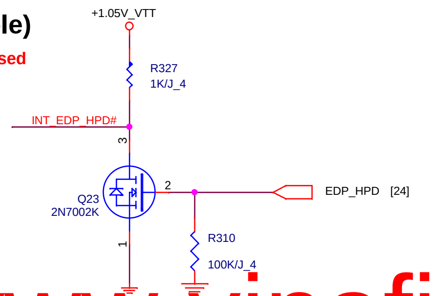
DP & PEG Compensation

CAD Note: Place PU resistor
within 2 inches of CPU



eDP Hot-plug (Disable)

HPD PU/PD resistor values based
on CRB and different to DG



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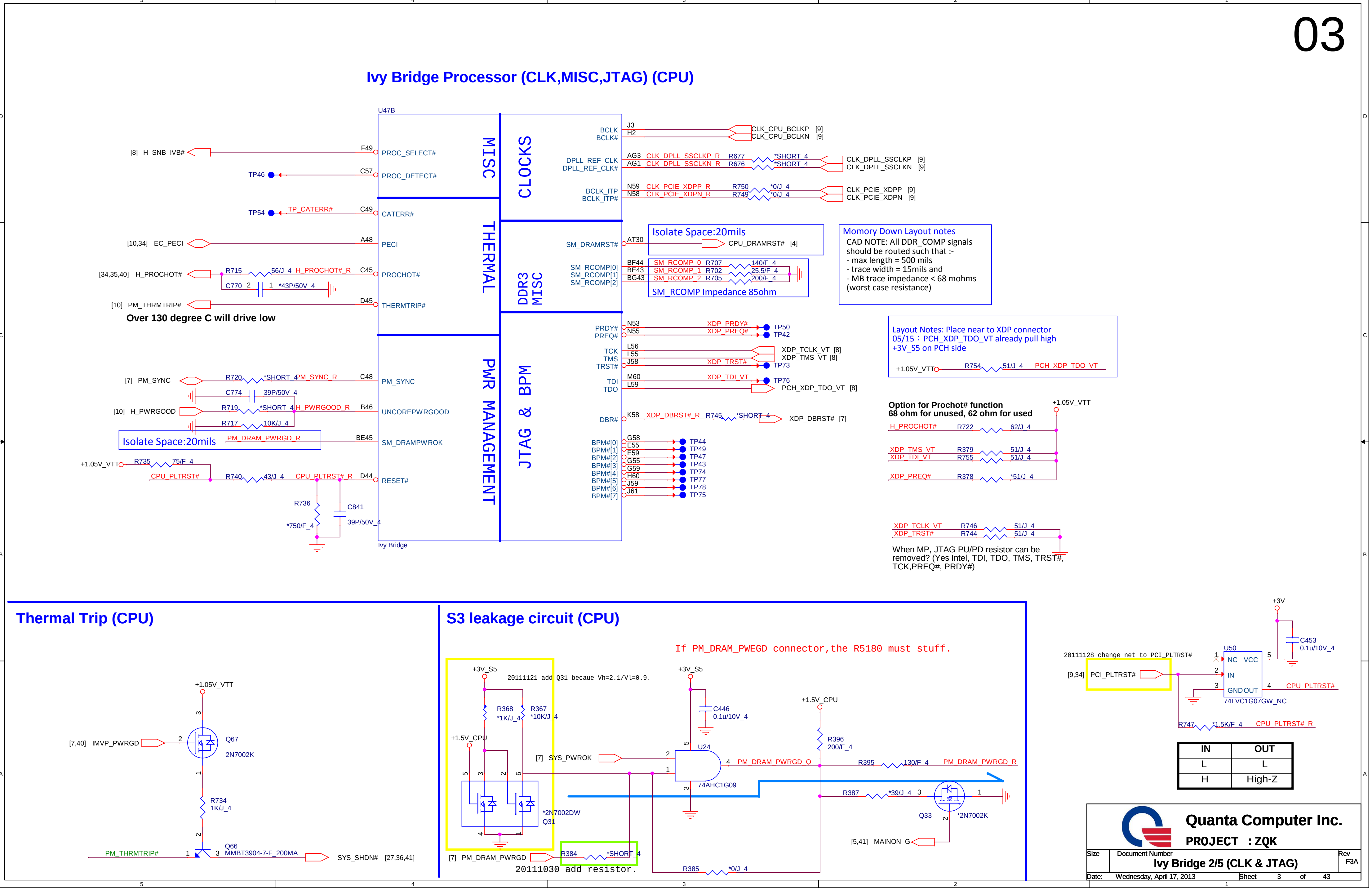
03
Ivy Bridge Processor (CLK,MISC,JTAG) (CPU)
U47B
MISC
CLOCKS
THERMAL
DDR3 MISC
PWR MANAGEMENT
JTAG & BPM
Ivy Bridge
[8] H_SNB_IVB#
F49 PROC_SELECT#
TP46
C57 PROC_DETECT#
TP54 TP_CATERR#
C49 CATERR#
[10,34] EC_PECI
A48 PECI
[34,35,40] H_PROCHOT#
R715 56/J_4 H_PROCHOT#_R
C45 PROCHOT#
C770 *43P/50V_4
[10] PM_THRMTRIP#
D45 THERMTRIP#
Over 130 degree C will drive low
[7] PM_SYNC
R720 *SHORT_4 PM_SYNC_R
C48 PM_SYNC
C774 39P/50V_4
[10] H_PWRGOOD
R719 *SHORT_4 H_PWRGOOD_R
B46 UNCOREPWRGOOD
R717 10K/J_4
Isolate Space:20mils
PM_DRAM_PWRGD_R
BE45 SM_DRAMPWROK
+1.05V_VTT
R735 75/F_4
CPU_PLTRST#
R740 43/J_4 CPU_PLTRST#_R
D44 RESET#
R736 *750/F_4
C841 39P/50V_4
BCLK J3
BCLK# H2
CLK_CPU_BCLKP [9]
CLK_CPU_BCLKN [9]
DPLL_REF_CLK AG3 CLK_DPLL_SSCLKP_R R677 *SHORT_4
DPLL_REF_CLK# AG1 CLK_DPLL_SSCLKN_R R676 *SHORT_4
CLK_DPLL_SSCLKP [9]
CLK_DPLL_SSCLKN [9]
BCLK_ITP N59 CLK_PCIE_XDPP_R R750 *0/J_4
BCLK_ITP# N58 CLK_PCIE_XDPN_R R749 *0/J_4
CLK_PCIE_XDPP [9]
CLK_PCIE_XDPN [9]
Isolate Space:20mils
SM_DRAMRST# AT30 CPU_DRAMRST# [4]
SM_RCOMP[0] BF44 SM_RCOMP_0 R707 140/F_4
SM_RCOMP[1] BE43 SM_RCOMP_1 R702 25.5/F_4
SM_RCOMP[2] BG43 SM_RCOMP_2 R705 200/F_4
SM_RCOMP Impedance 85ohm
Momory Down Layout notes
CAD NOTE: All DDR_COMP signals should be routed such that :-
- max length = 500 mils
- trace width = 15mils and
- MB trace impedance < 68 mohms
(worst case resistance)
PRDY# N53 XDP_PRDY# TP50
PREQ# N55 XDP_PREQ# TP42
TCK L56 XDP_TCLK_VT [8]
TMS L55 XDP_TMS_VT [8]
TRST# J58 XDP_TRST# TP73
TDI M60 XDP_TDI_VT TP76
TDO L59 PCH_XDP_TDO_VT [8]
DBR# K58 XDP_DBRST#_R R745 *SHORT_4 XDP_DBRST# [7]
BPM#[0] G58 TP44
BPM#[1] E55 TP49
BPM#[2] E59 TP47
BPM#[3] G55 TP43
BPM#[4] G59 TP74
BPM#[5] H60 TP77
BPM#[6] J59 TP78
BPM#[7] J61 TP75
Layout Notes: Place near to XDP connector
05/15 : PCH_XDP_TDO_VT already pull high
+3V_S5 on PCH side
+1.05V_VTT R754 51/J_4 PCH_XDP_TDO_VT
Option for Prochot# function
68 ohm for unused, 62 ohm for used
+1.05V_VTT
H_PROCHOT# R722 62/J_4
XDP_TMS_VT R379 51/J_4
XDP_TDI_VT R755 51/J_4
XDP_PREQ# R378 *51/J_4
XDP_TCLK_VT R746 51/J_4
XDP_TRST# R744 51/J_4
When MP, JTAG PU/PD resistor can be removed? (Yes Intel, TDI, TDO, TMS, TRST#, TCK,PREQ#, PRDY#)
Thermal Trip (CPU)
+1.05V_VTT
[7,40] IMVP_PWRGD
Q67 2N7002K
R734 1K/J_4
PM_THRMTRIP#
Q66 MMBT3904-7-F_200MA
SYS_SHDN# [27,36,41]
S3 leakage circuit (CPU)
If PM_DRAM_PWEGD connector,the R5180 must stuff.
+3V_S5
20111121 add Q31 becaue Vh=2.1/Vl=0.9.
R368 *1K/J_4
R367 *10K/J_4
+1.5V_CPU
*2N7002DW Q31
[7] SYS_PWROK
+3V_S5
C446 0.1u/10V_4
U24 74AHC1G09
PM_DRAM_PWRGD_Q
+1.5V_CPU
R396 200/F_4
R395 130/F_4 PM_DRAM_PWRGD_R
R387 *39/J_4
Q33 *2N7002K
[5,41] MAINON_G
[7] PM_DRAM_PWRGD
R384 *SHORT_4
20111030 add resistor.
R385 *0/J_4
+3V
C453 0.1u/10V_4
20111128 change net to PCI_PLTRST#
U50 74LVC1G07GW_NC
NC VCC
IN
GND OUT
[9,34] PCI_PLTRST#
CPU_PLTRST#
R747 *1.5K/F_4 CPU_PLTRST#_R
IN OUT
L L
H High-Z
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Ivy Bridge 2/5 (CLK & JTAG)
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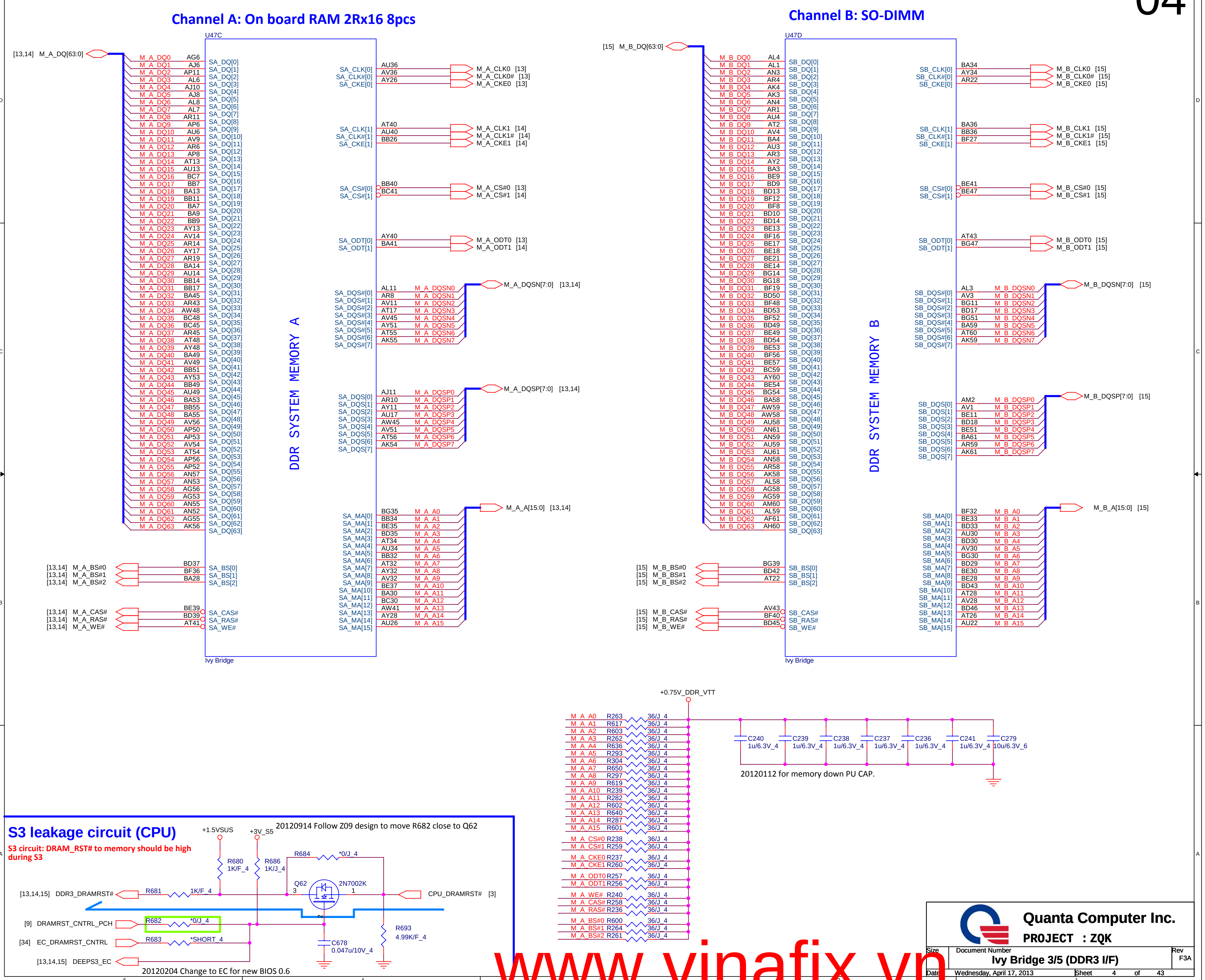
Ivy Bridge Processor (CPU)

04



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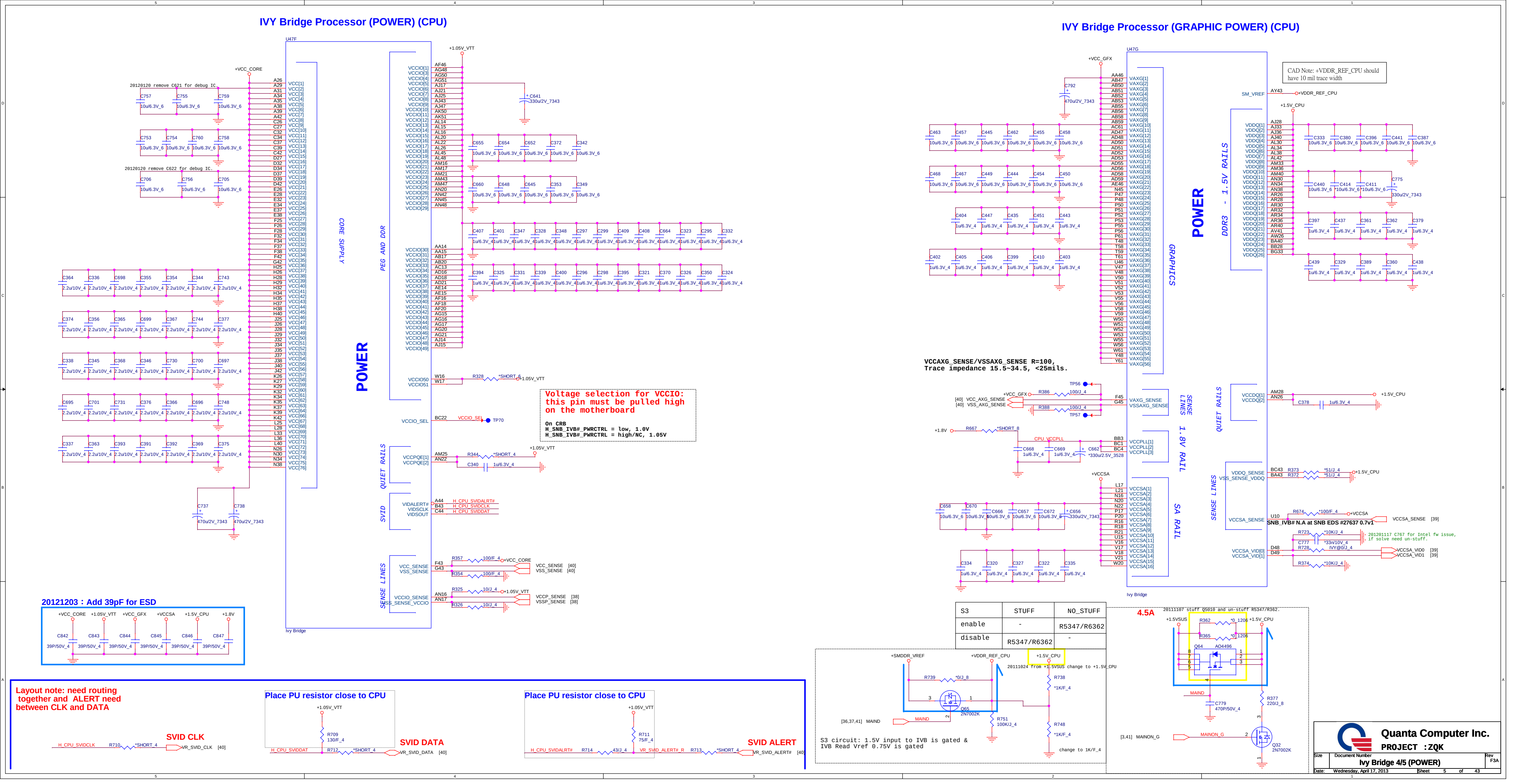

IVY Bridge Processor (POWER) (CPU)
IVY Bridge Processor (GRAPHIC POWER) (CPU)
U47F
U47G
+VCC_CORE
+1.05V_VTT
+VCC_GFX
+1.5V_CPU
+VCCSA
20120120 remove C621 for debug IC.
20120120 remove C622 for debug IC.
CORE SUPPLY
PEG AND DDR
POWER
QUIET RAILS
SVID
SENSE LINES
GRAPHICS
DDR3 - 1.5V RAILS
1.8V RAIL
SA RAIL
CAD Note: +VDDR_REF_CPU should have 10 mil trace width
VCCAXG_SENSE/VSSAXG_SENSE R=100, Trace impedance 15.5~34.5, <25mils.
Voltage selection for VCCIO: this pin must be pulled high on the motherboard
On CRB
H_SNB_IVB#_PWRCTRL = low, 1.0V
H_SNB_IVB#_PWRCTRL = high/NC, 1.05V
SNB_IVB# N.A at SNB EDS #27637 0.7v1
20121117 C767 for Intel fw issue, if solve need un-stuff.
20121203 : Add 39pF for ESD
Layout note: need routing together and ALERT need between CLK and DATA
Place PU resistor close to CPU
SVID CLK
SVID DATA
SVID ALERT
4.5A
20111107 stuff Q5010 and un-stuff R5347/R6362.
20111024 from +1.5VSUS change to +1.5V_CPU
S3 circuit: 1.5V input to IVB is gated & IVB Read Vref 0.75V is gated
S3 | STUFF | NO_STUFF
enable | - | R5347/R6362
disable | R5347/R6362 | -
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Ivy Bridge 4/5 (POWER)
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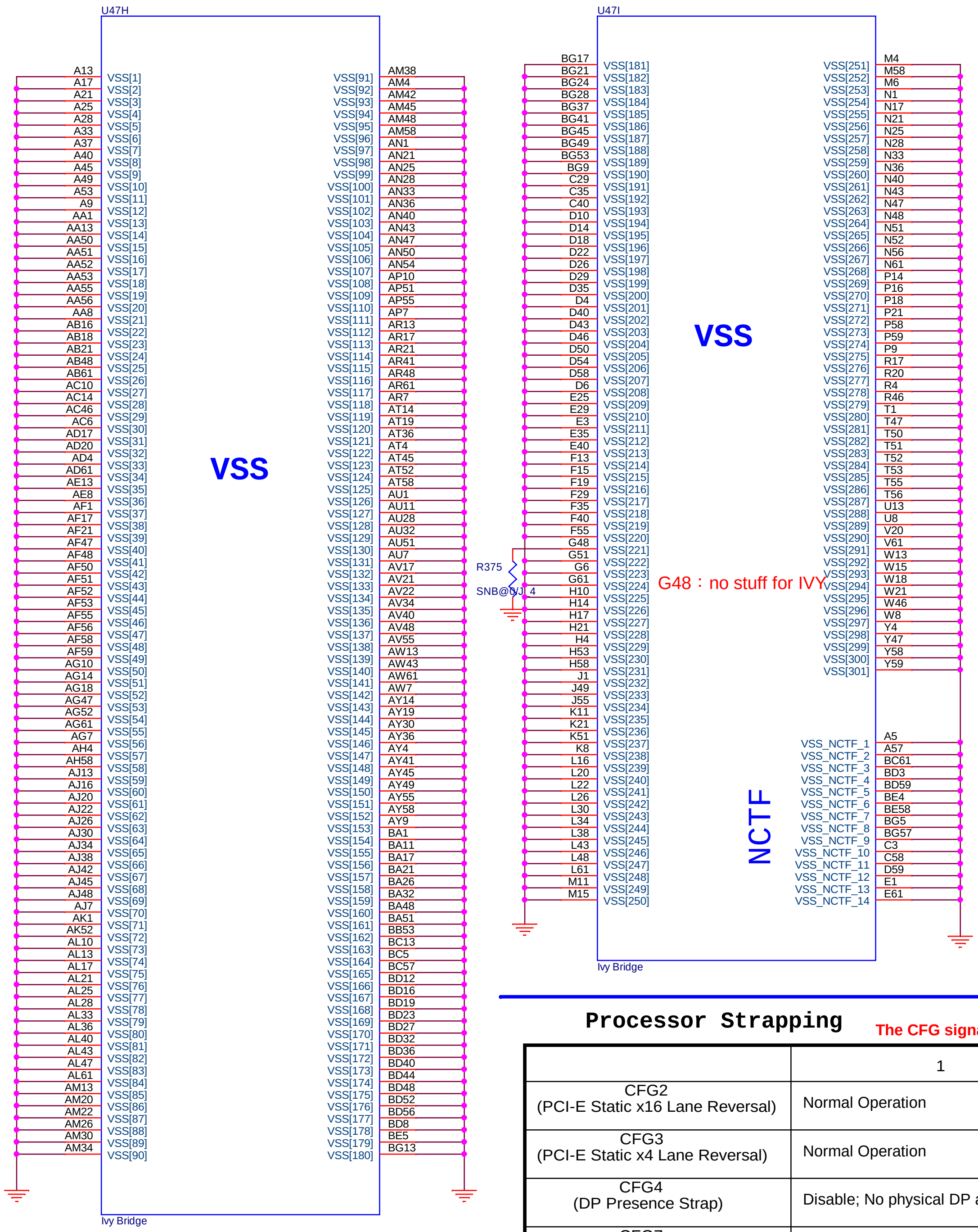
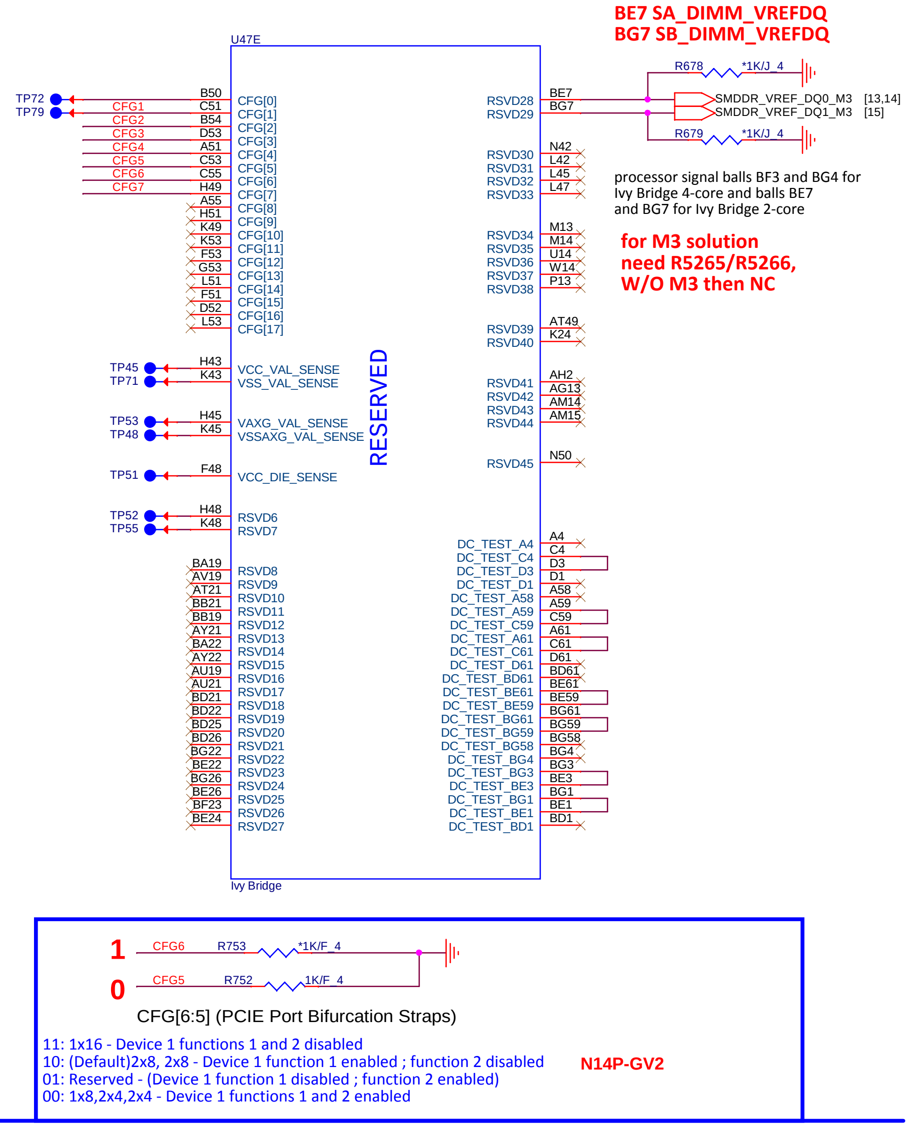
IVY Bridge Processor (GND) (CPU)



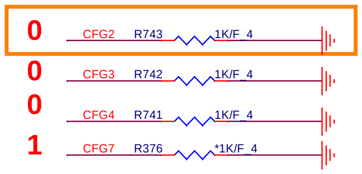
IVY Bridge Processor (RESERVED, CFG) (CPU)

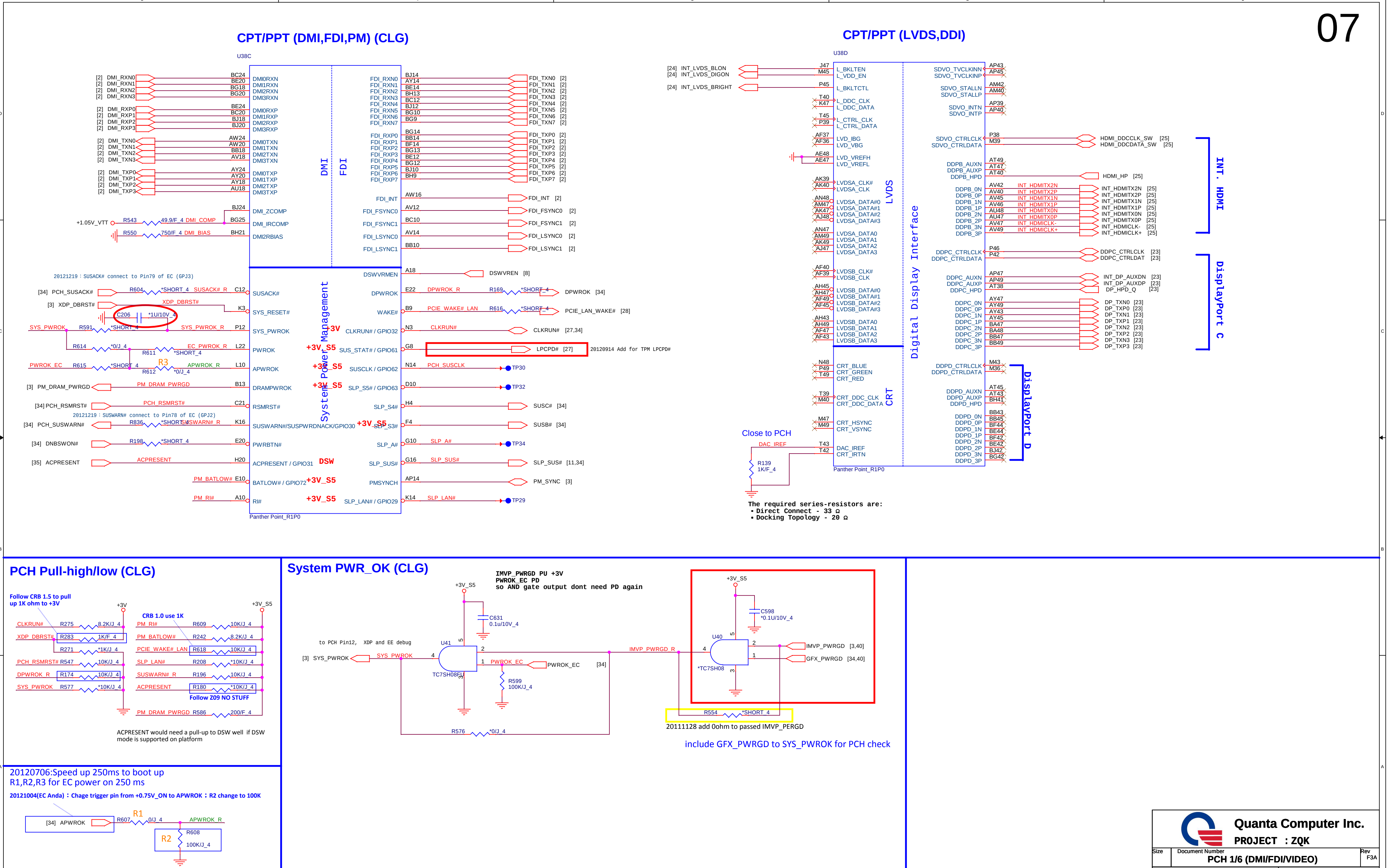


Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PCI-E Static x16 Lane Reversal)	Normal Operation	Lane Reversed
CFG3 (PCI-E Static x4 Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training





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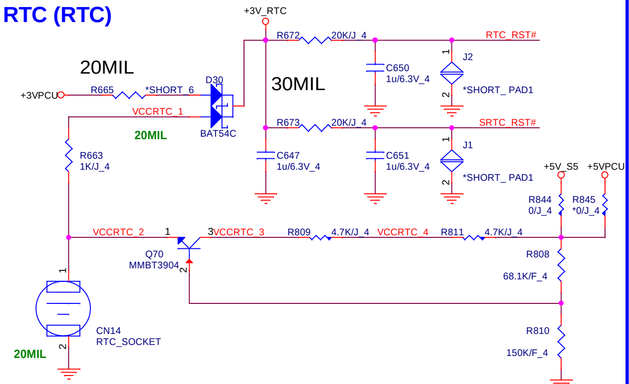
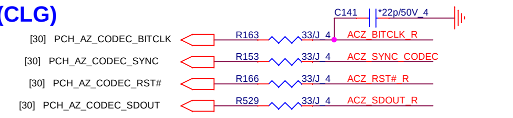
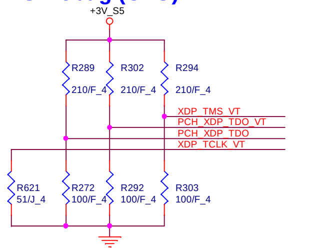
RTC (RTC)



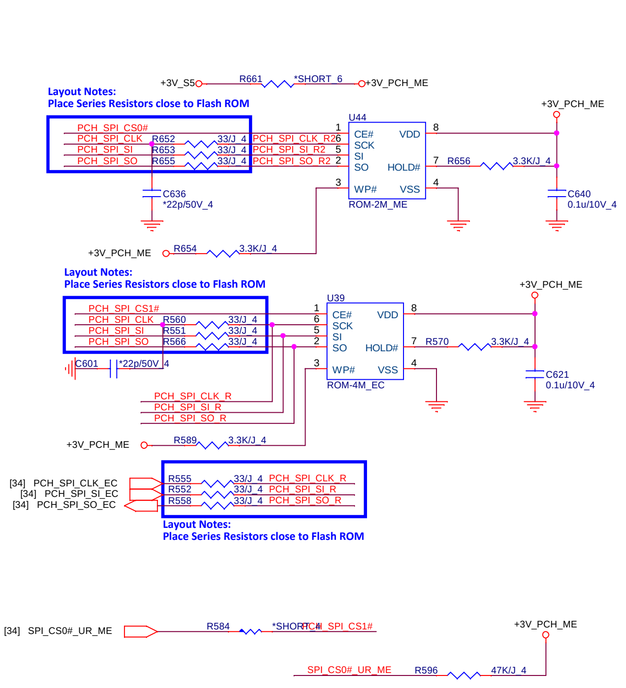
HDA Bus (CLG)



PCH JTAG Debug (CLG)

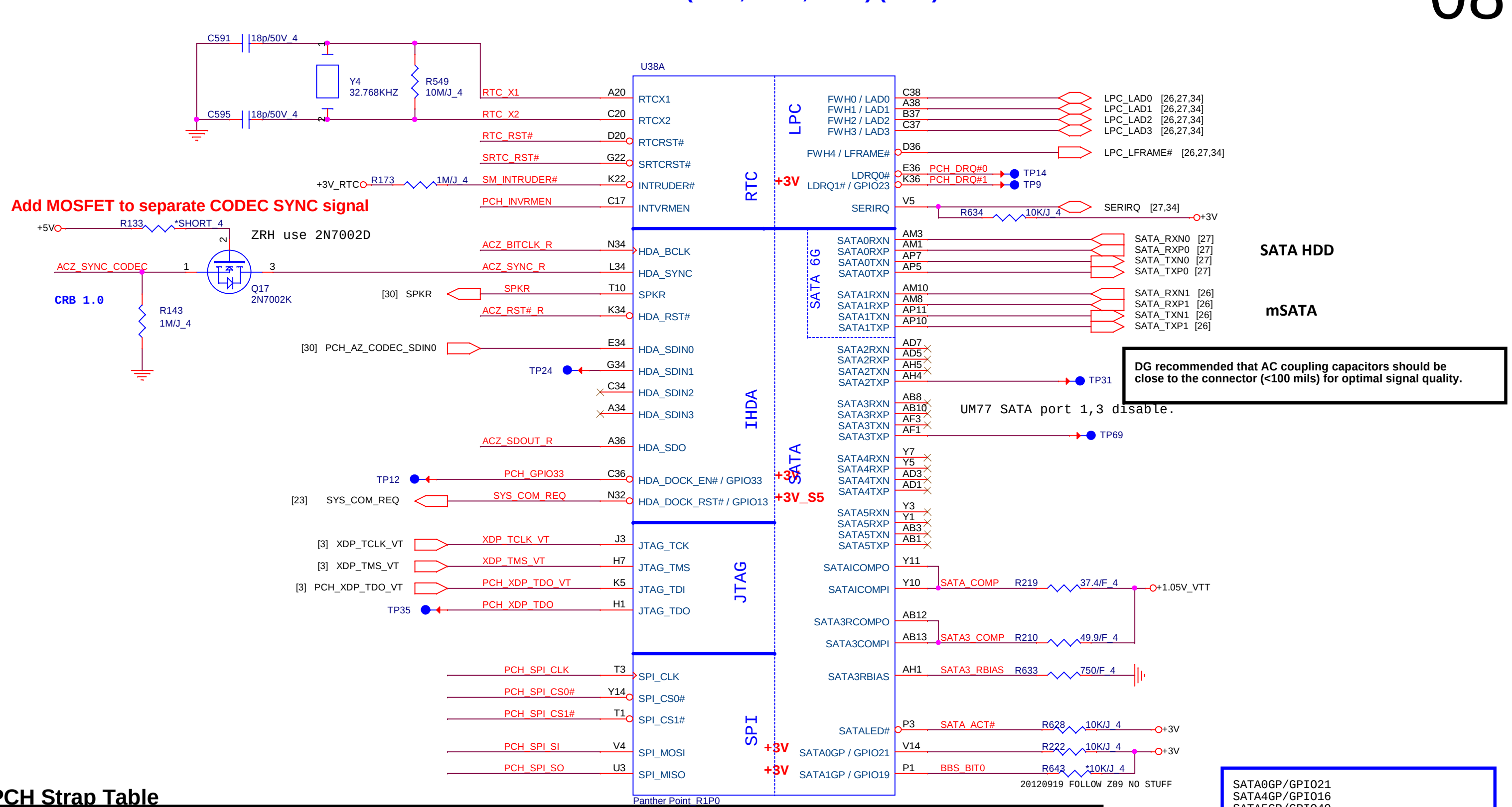


PCH Dual SPI (CLG) (Default for WIN8)



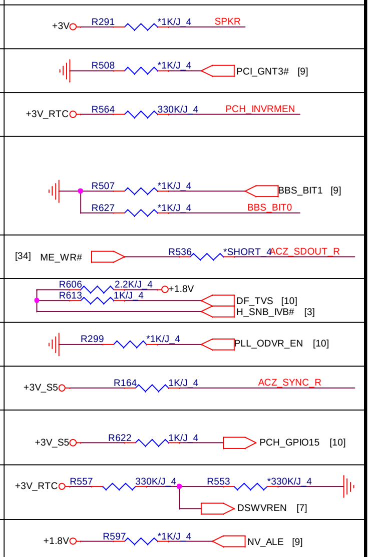
PCH2 (CLG)

CPT/PPT (HDA,JTAG,SATA) (CLG)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GPIO19 / Boot Location: 1 / 1 / SPI * 0 / 0 / LPC
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	
HDA_SDO	Flash Descriptor Security	RSMRST	0 = effect (default)(weak pull-down 20K) 1 = overridden
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss (weak pull-down 20K) 1 = Set to Vcc
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (weak pull-up 10K)
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V
GPIO15	Intel ME Crypto Transport Layer Security (TLS) cipher suite internal PD	RSMRST	0 = Disable (Default) 1 = Enable
DSWVREN	DEEP S4/S5 well On Die DSW VR Enable	DSW	High = Enable (Default) Low = Disable
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)



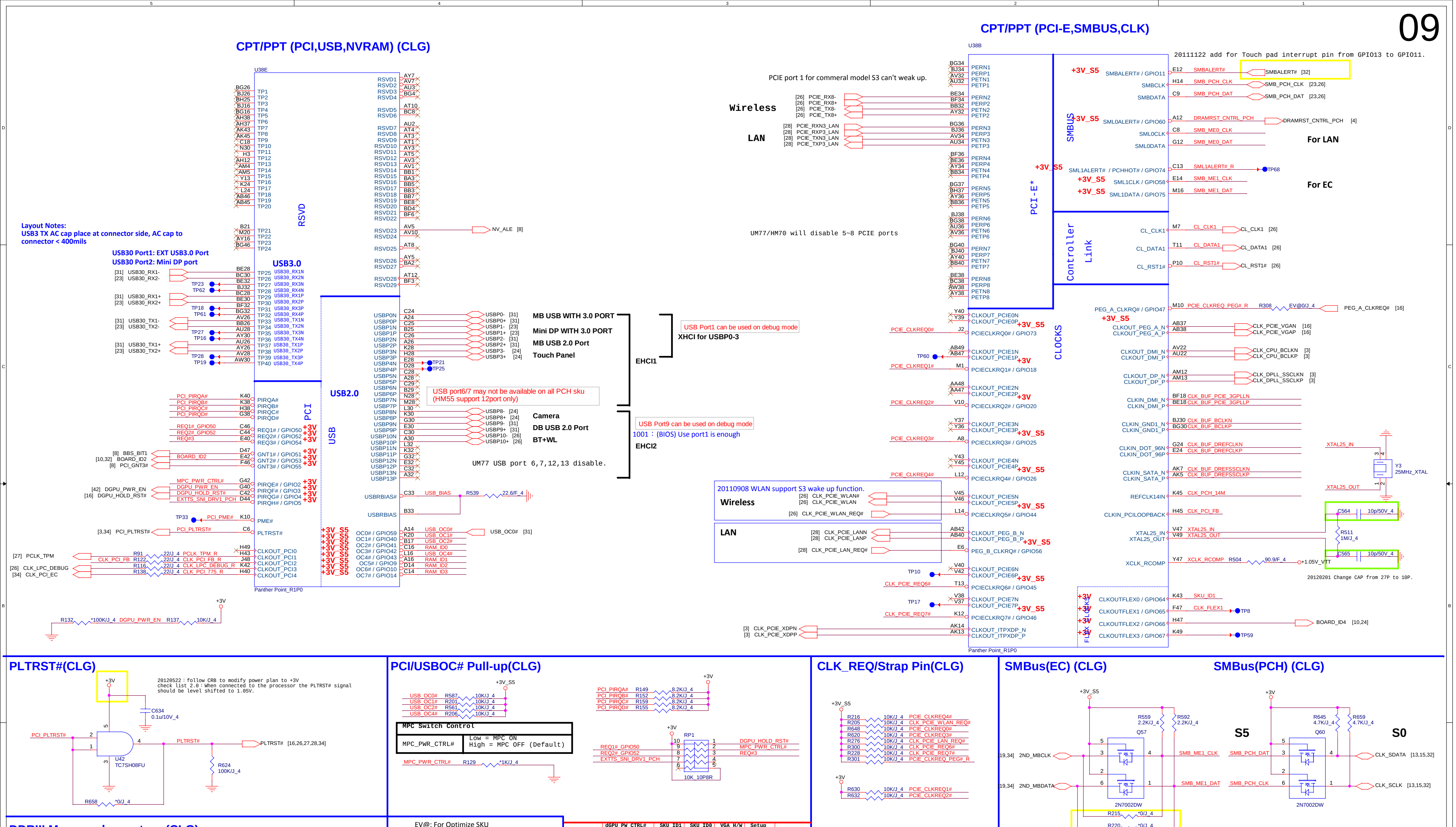
Used as GPIO only. at chklist 1.2

Default weak pull-up on GNT0/1#
[Need external pull-down for LPC BIOS]

ME_WR default EC setting folating

for future CPU, Sandy Bridge NC
DF_TVS needs to be pulled up to VccDFTERM power rail through 2.2 kOhm ±5% - R8361 change to 0 or not??

Needs to be pulled High for Chief River platform
chklist 2.0



MPC Switch Control

MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

	dGPU_PW_CTRL# (GPIO68) CTL : dGPU_VRON	SKU_ID1 (GPIO64)	SKU_ID0 (GPIO16)	VGA H/W Signal	Setup Menu	
UMA Only	1	0	0	UMA	Hidden	UMA boot
dGPU Only	0 or 1	0	1	GPU	Hidden	GPU boot
Switchable (Mux)	0	1	0	UMA+GPU	dGPU/SG	UMA boot
Optimize (Muxless)	0	1	1	UMA	UMA/SG	UMA boot

dGPU_PW_CTRL#
1 = GPU power is control by H/W (pure Discrete SKU)
0 = GPU power is control by PCH GPIO (Discrete, SG or Optimize)

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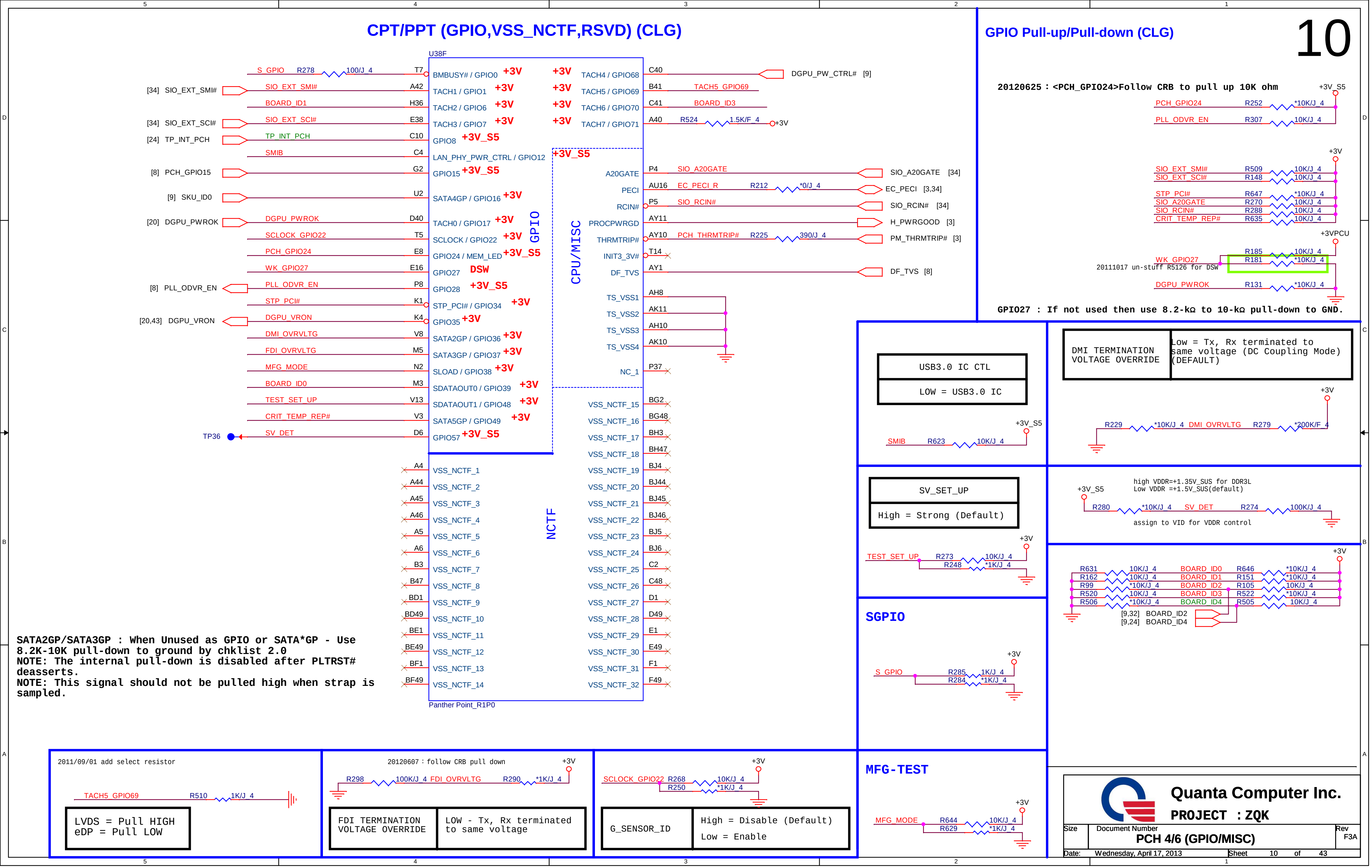
CPT/PPT (GPIO,VSS_NCTF,RSVD) (CLG)
U38F
GPIO
CPU/MISC
NCTF
Panther Point_R1P0
S_GPIO R278 100/J_4 T7 BMBUSY# / GPIO0 +3V
[34] SIO_EXT_SMI# A42 TACH1 / GPIO1 +3V
BOARD_ID1 H36 TACH2 / GPIO6 +3V
[34] SIO_EXT_SCI# E38 TACH3 / GPIO7 +3V
[24] TP_INT_PCH C10 GPIO8 +3V_S5
SMIB C4 LAN_PHY_PWR_CTRL / GPIO12 +3V_S5
[8] PCH_GPIO15 G2 GPIO15 +3V_S5
[9] SKU_ID0 U2 SATA4GP / GPIO16 +3V
[20] DGPU_PWROK D40 TACH0 / GPIO17 +3V
SCLOCK_GPIO22 T5 SCLOCK / GPIO22 +3V
PCH_GPIO24 E8 GPIO24 / MEM_LED +3V_S5
WK_GPIO27 E16 GPIO27 DSW
[8] PLL_ODVR_EN P8 GPIO28 +3V_S5
STP_PCI# K1 STP_PCI# / GPIO34 +3V
[20,43] DGPU_VRON K4 GPIO35 +3V
DMI_OVRVLTG V8 SATA2GP / GPIO36 +3V
FDI_OVRVLTG M5 SATA3GP / GPIO37 +3V
MFG_MODE N2 SLOAD / GPIO38 +3V
BOARD_ID0 M3 SDATAOUT0 / GPIO39 +3V
TEST_SET_UP V13 SDATAOUT1 / GPIO48 +3V
CRIT_TEMP_REP# V3 SATA5GP / GPIO49 +3V
TP36 SV_DET D6 GPIO57 +3V_S5
+3V TACH4 / GPIO68 C40 DGPU_PW_CTRL# [9]
+3V TACH5 / GPIO69 B41 TACH5_GPIO69
+3V TACH6 / GPIO70 C41 BOARD_ID3
+3V TACH7 / GPIO71 A40 R524 1.5K/F_4 +3V
A20GATE P4 SIO_A20GATE SIO_A20GATE [34]
PECI AU16 EC_PECI_R R212 *0/J_4 EC_PECI [3,34]
RCIN# P5 SIO_RCIN# SIO_RCIN# [34]
PROCPWRGD AY11 H_PWRGOOD [3]
THRMTRIP# AY10 PCH_THRMTRIP# R225 390/J_4 PM_THRMTRIP# [3]
INIT3_3V# T14
DF_TVS AY1 DF_TVS [8]
TS_VSS1 AH8
TS_VSS2 AK11
TS_VSS3 AH10
TS_VSS4 AK10
NC_1 P37
VSS_NCTF_1 A4 … VSS_NCTF_14 BF49
VSS_NCTF_15 BG2 … VSS_NCTF_32 F49
SATA2GP/SATA3GP : When Unused as GPIO or SATA*GP - Use 8.2K-10K pull-down to ground by chklist 2.0
NOTE: The internal pull-down is disabled after PLTRST# deasserts.
NOTE: This signal should not be pulled high when strap is sampled.
2011/09/01 add select resistor
TACH5_GPIO69 R510 1K/J_4
LVDS = Pull HIGH
eDP = Pull LOW
20120607 : follow CRB pull down
R298 100K/J_4 FDI_OVRVLTG R290 *1K/J_4 +3V
FDI TERMINATION VOLTAGE OVERRIDE
LOW - Tx, Rx terminated to same voltage
SCLOCK_GPIO22 R268 10K/J_4 R250 *1K/J_4 +3V
G_SENSOR_ID
High = Disable (Default)
Low = Enable
GPIO Pull-up/Pull-down (CLG)
10
20120625 : <PCH_GPIO24>Follow CRB to pull up 10K ohm
PCH_GPIO24 R252 *10K/J_4 +3V_S5
PLL_ODVR_EN R307 10K/J_4
SIO_EXT_SMI# R509 10K/J_4 +3V
SIO_EXT_SCI# R148 10K/J_4
STP_PCI# R647 *10K/J_4
SIO_A20GATE R270 10K/J_4
SIO_RCIN# R288 10K/J_4
CRIT_TEMP_REP# R635 10K/J_4
WK_GPIO27 R185 10K/J_4 R181 *10K/J_4 +3VPCU
20111017 un-stuff R5126 for DSW
DGPU_PWROK R131 *10K/J_4
GPIO27 : If not used then use 8.2-kΩ to 10-kΩ pull-down to GND.
USB3.0 IC CTL
LOW = USB3.0 IC
SMIB R623 10K/J_4 +3V_S5
DMI TERMINATION VOLTAGE OVERRIDE
Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)
R229 *10K/J_4 DMI_OVRVLTG R279 *200K/F_4 +3V
SV_SET_UP
High = Strong (Default)
TEST_SET_UP R273 10K/J_4 R248 *1K/J_4 +3V
high VDDR=+1.35V_SUS for DDR3L
Low VDDR =+1.5V_SUS(default)
+3V_S5 R280 *10K/J_4 SV_DET R274 100K/J_4
assign to VID for VDDR control
R631 10K/J_4 BOARD_ID0 R646 *10K/J_4
R162 10K/J_4 BOARD_ID1 R151 *10K/J_4
R99 *10K/J_4 BOARD_ID2 R105 10K/J_4
R520 10K/J_4 BOARD_ID3 R522 *10K/J_4
R506 *10K/J_4 BOARD_ID4 R505 10K/J_4
[9,32] BOARD_ID2
[9,24] BOARD_ID4
SGPIO
S_GPIO R285 1K/J_4 R284 *1K/J_4 +3V
MFG-TEST
MFG_MODE R644 10K/J_4 R629 *1K/J_4 +3V
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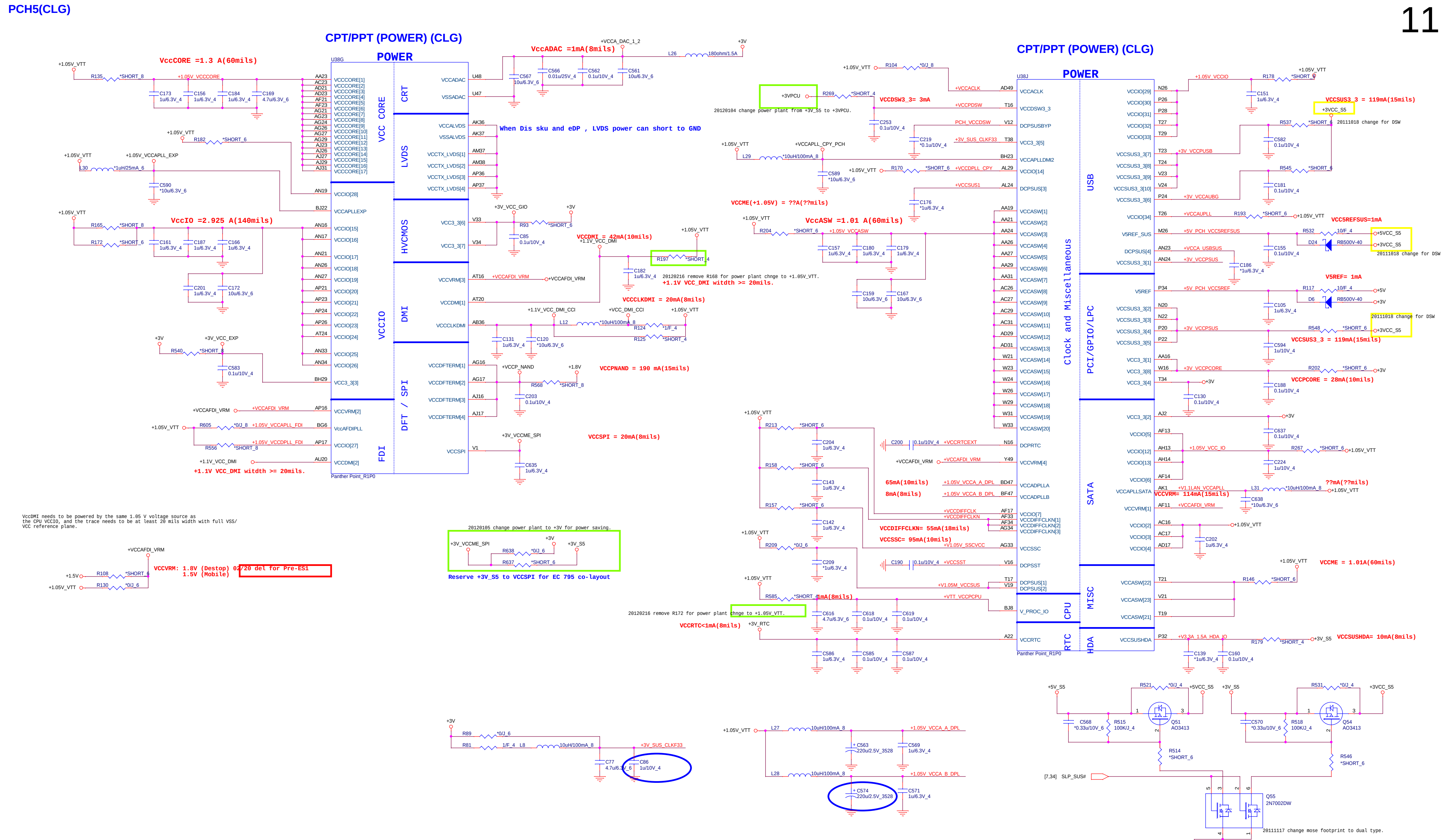

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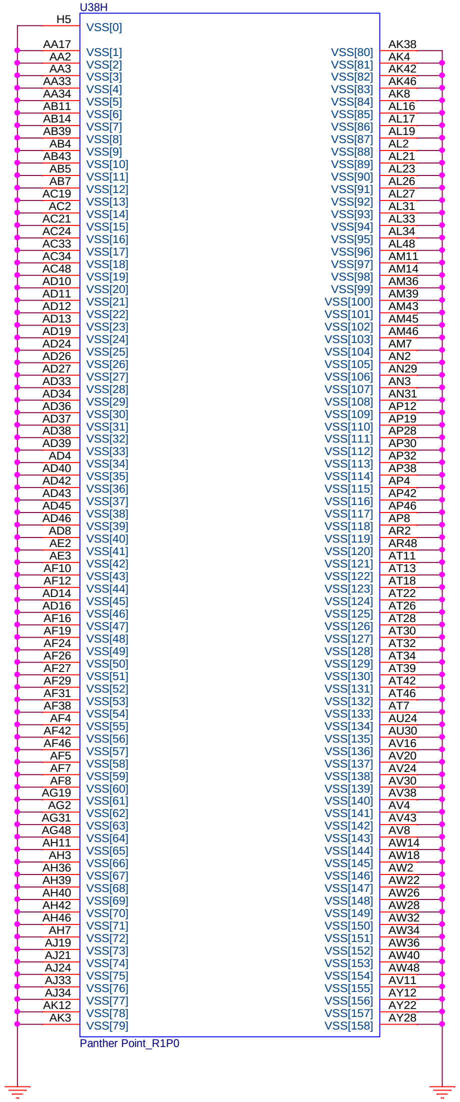
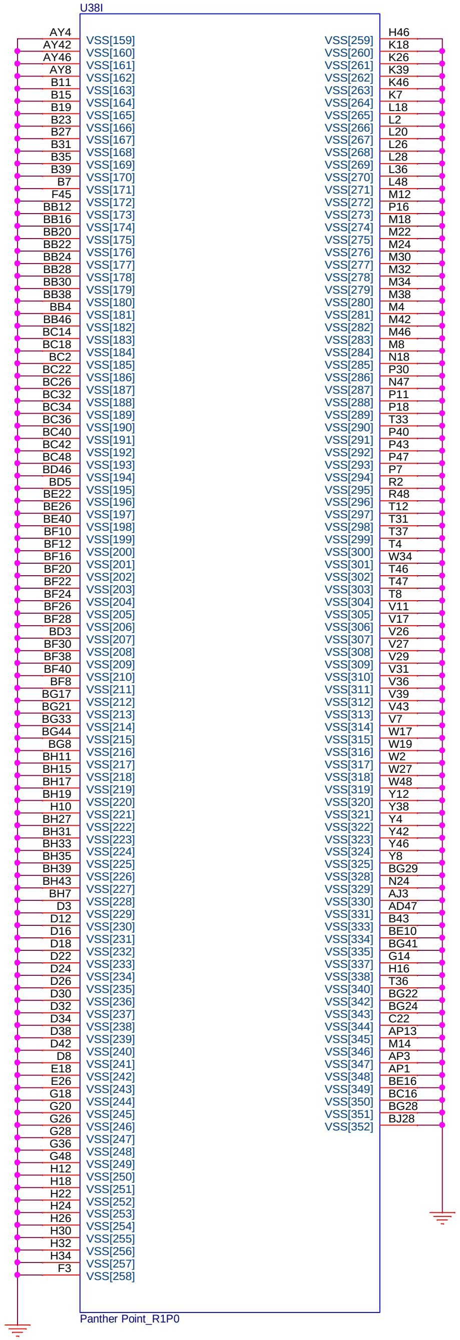
PCH6(CLG)

IBEX PEAK-M (GND) (CLG)





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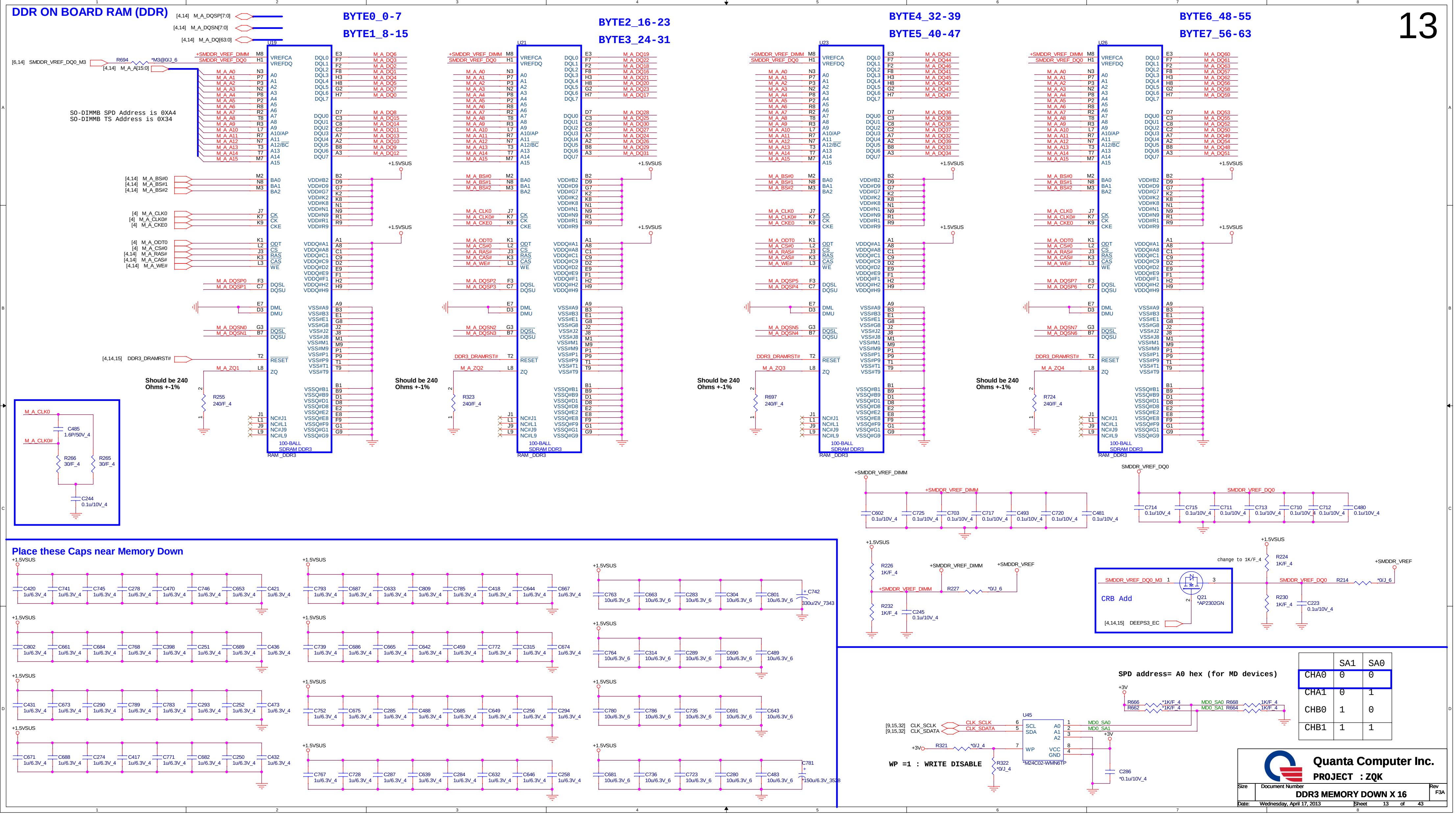
PROJECT :ZQK

Size	Document Number	Rev
	PCH 6/6 (GND)	F3A
Date:	Wednesday, April 17, 2013	Sheet 12 of 43



	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

Quanta Computer Inc.

PROJECT : ZQK

Size	Document Number	Rev
	DDR3 MEMORY DOWN X 16	F3A
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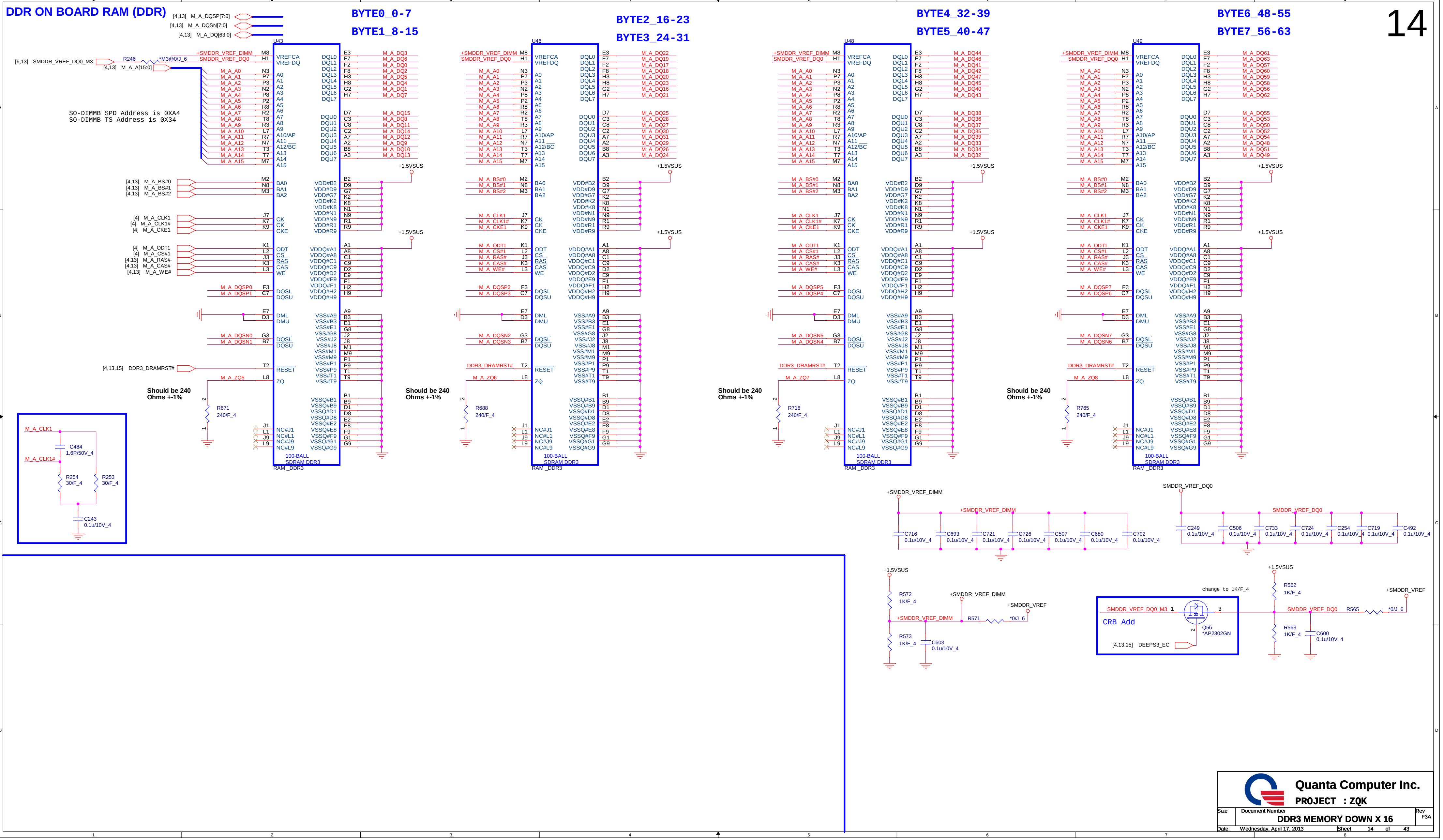
DDR ON BOARD RAM (DDR)



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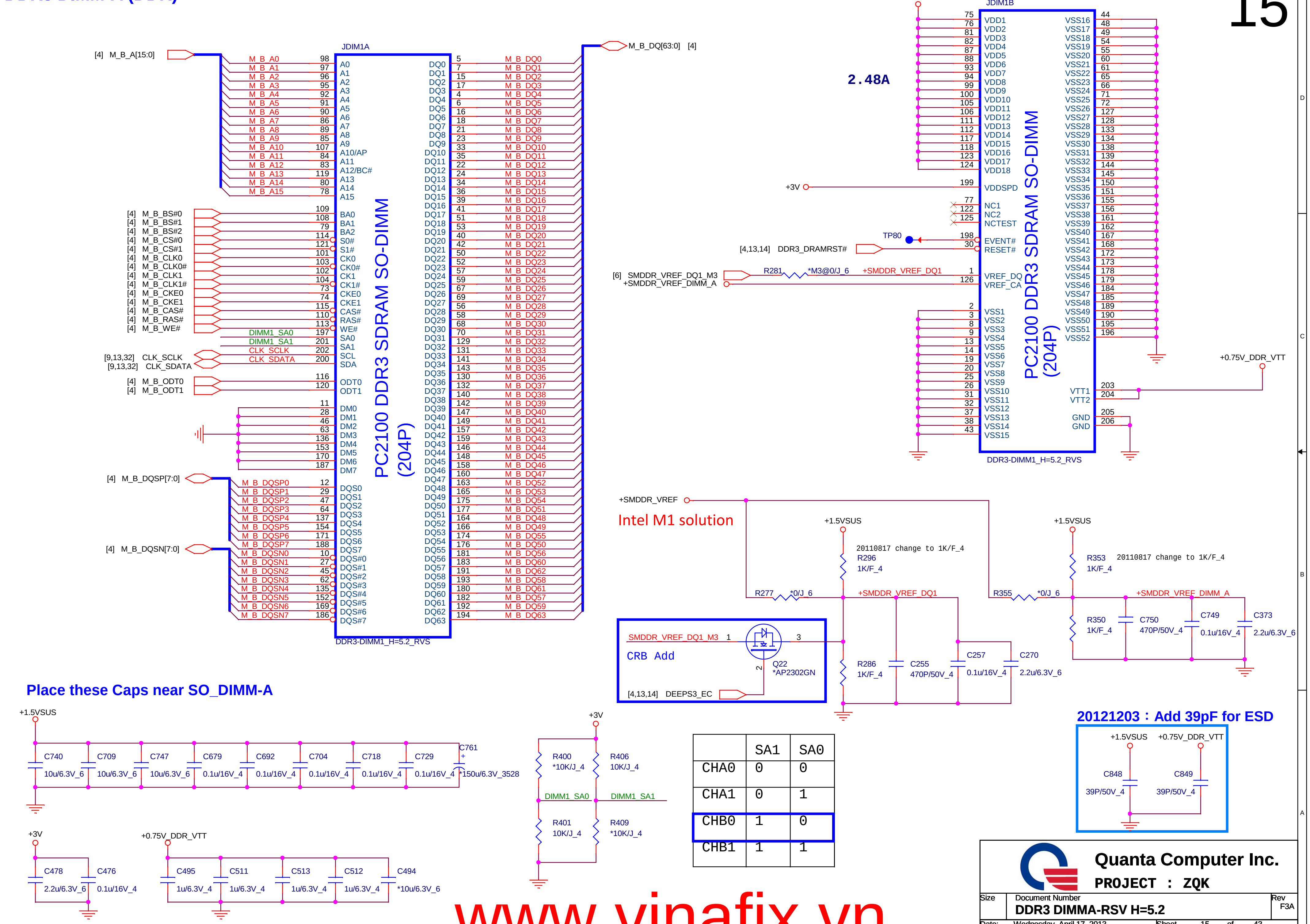
PROJECT : ZQK

Size	Document Number	Rev
	DDR3 MEMORY DOWN X 16	F3A

Date: Wednesday, April 17, 2013 Sheet 14 of 43

DDR3 DIMM-A (DDR)



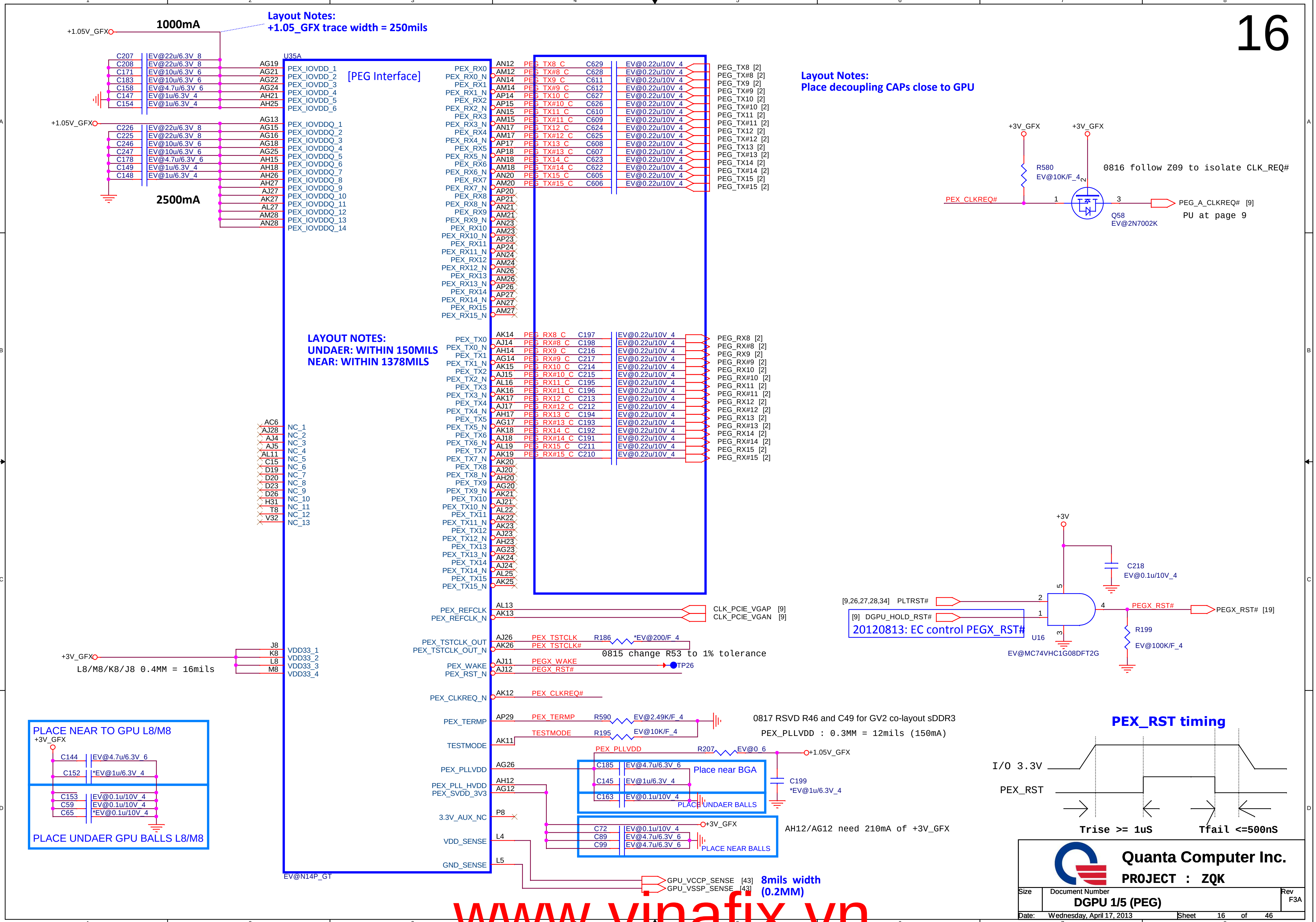
	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

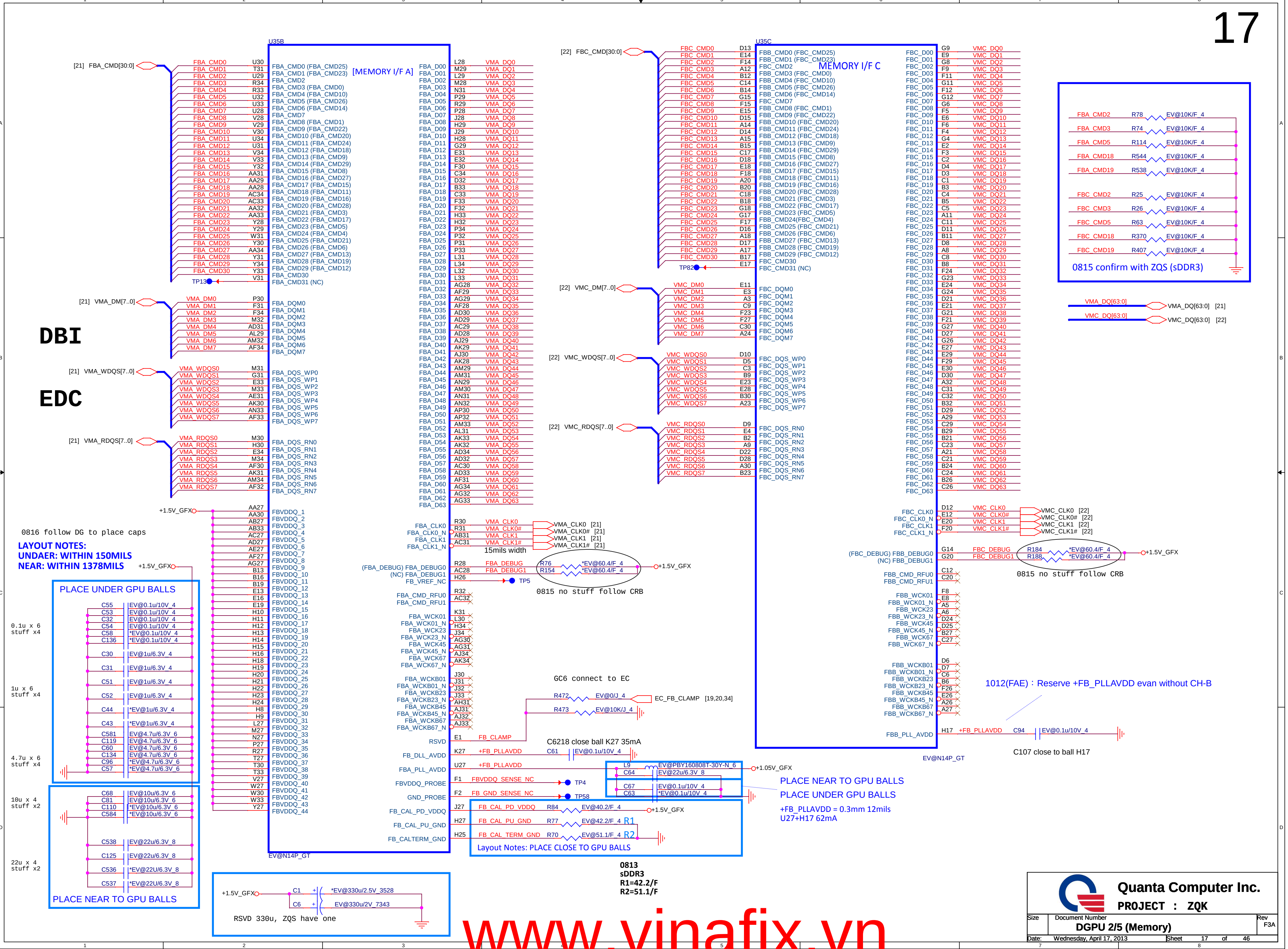
Quanta Computer Inc.

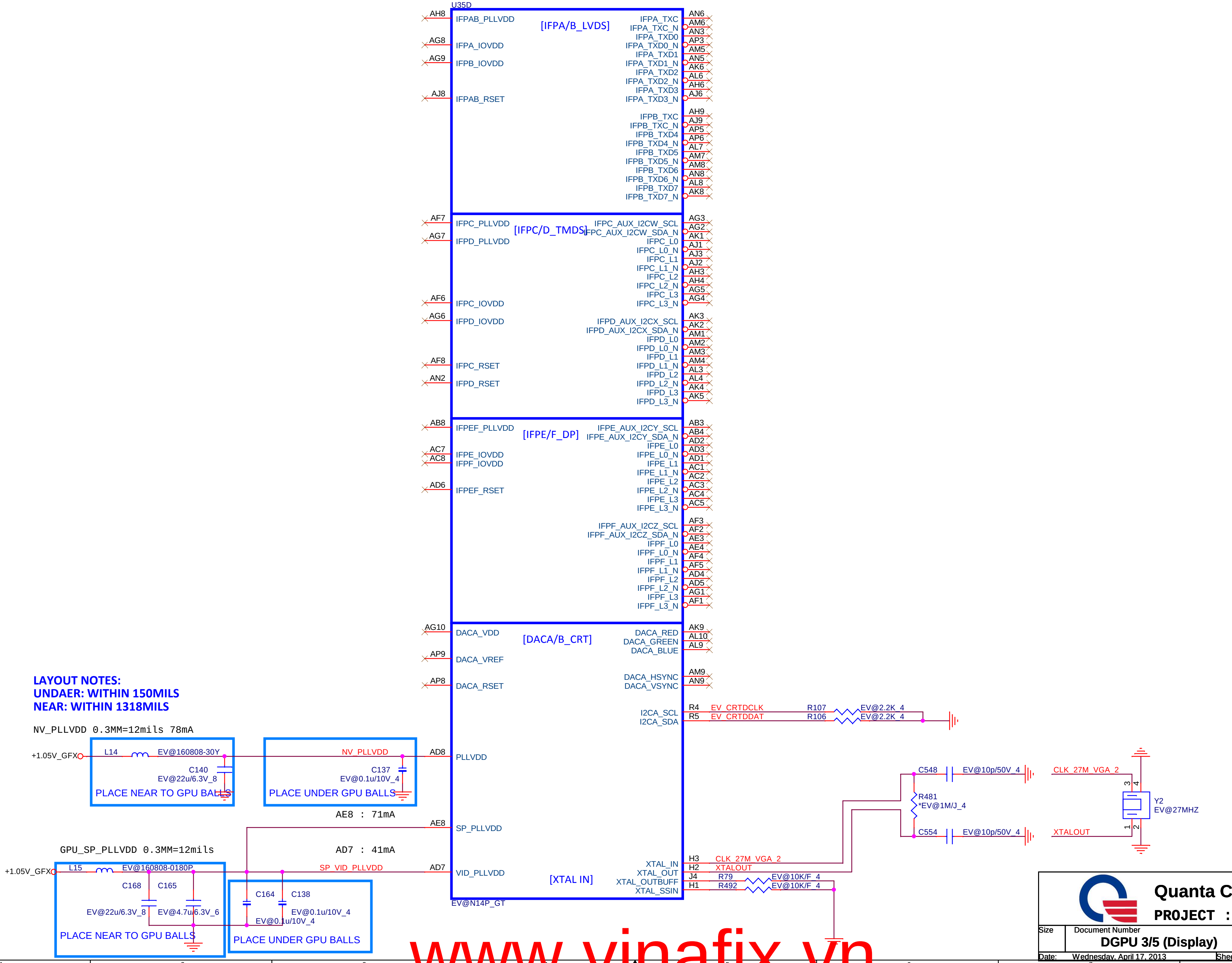
PROJECT : ZQK

Size	Document Number	Rev
	DDR3 DIMMA-RSV H=5.2	F3A

Date: Wednesday, April 17, 2013 Sheet 15 of 43


Layout Notes:
+1.05_GFX trace width = 250mils
+1.05V_GFX
1000mA
2500mA
U35A
[PEG Interface]
C207 EV@22u/6.3V_8
C208 EV@22u/6.3V_8
C171 EV@10u/6.3V_6
C183 EV@10u/6.3V_6
C158 EV@4.7u/6.3V_6
C147 EV@1u/6.3V_4
C154 EV@1u/6.3V_4
C226 EV@22u/6.3V_8
C225 EV@22u/6.3V_8
C246 EV@10u/6.3V_6
C247 EV@10u/6.3V_6
C178 EV@4.7u/6.3V_6
C149 EV@1u/6.3V_4
C148 EV@1u/6.3V_4
PEX_IOVDD_1 ... PEX_IOVDD_6
PEX_IOVDDQ_1 ... PEX_IOVDDQ_14
PEX_RX0 ... PEX_RX15_N
PEX_TX0 ... PEX_TX15_N
PEG_TX8 ... PEG_TX#15 [2]
EV@0.22u/10V_4
PEG_RX8 ... PEG_RX#15 [2]
Layout Notes:
Place decoupling CAPs close to GPU
LAYOUT NOTES:
UNDAER: WITHIN 150MILS
NEAR: WITHIN 1378MILS
NC_1 ... NC_13
+3V_GFX
R580 EV@10K/F_4
0816 follow Z09 to isolate CLK_REQ#
PEX_CLKREQ#
Q58 EV@2N7002K
PEG_A_CLKREQ# [9]
PU at page 9
+3V
C218 EV@0.1u/10V_4
[9,26,27,28,34] PLTRST#
[9] DGPU_HOLD_RST#
20120813: EC control PEGX_RST#
U16 EV@MC74VHC1G08DFT2G
PEGX_RST#
PEGX_RST# [19]
R199 EV@100K/F_4
PEX_REFCLK
PEX_REFCLK_N
CLK_PCIE_VGAP [9]
CLK_PCIE_VGAN [9]
PEX_TSTCLK_OUT
PEX_TSTCLK_OUT_N
R186 *EV@200/F_4
0815 change R53 to 1% tolerance
PEX_WAKE
PEX_RST_N
PEGX_WAKE
PEGX_RST#
TP26
+3V_GFX
VDD33_1 ... VDD33_4
L8/M8/K8/J8 0.4MM = 16mils
PEX_CLKREQ_N
PEX_TERMP
R590 EV@2.49K/F_4
0817 RSVD R46 and C49 for GV2 co-layout sDDR3
TESTMODE
R195 EV@10K/F_4
PEX_PLLVDD : 0.3MM = 12mils (150mA)
PEX_PLLVDD
R207 EV@0_6
+1.05V_GFX
PEX_PLL_HVDD
PEX_SVDD_3V3
C185 EV@4.7u/6.3V_6
C145 EV@1u/6.3V_4
C163 EV@0.1u/10V_4
Place near BGA
PLACE UNDAER BALLS
C199 *EV@1u/6.3V_4
3.3V_AUX_NC
VDD_SENSE
GND_SENSE
C72 EV@0.1u/10V_4
C89 EV@4.7u/6.3V_6
C99 EV@4.7u/6.3V_6
PLACE NEAR BALLS
AH12/AG12 need 210mA of +3V_GFX
EV@N14P_GT
GPU_VCCP_SENSE [43]
GPU_VSSP_SENSE [43]
8mils width
(0.2MM)
PLACE NEAR TO GPU L8/M8
C144 EV@4.7u/6.3V_6
C152 *EV@1u/6.3V_4
C153 EV@0.1u/10V_4
C59 EV@0.1u/10V_4
C65 *EV@0.1u/10V_4
PLACE UNDAER GPU BALLS L8/M8
PEX_RST timing
I/O 3.3V
PEX_RST
Trise >= 1uS
Tfail <=500nS
Quanta Computer Inc.
PROJECT : ZQK
Size
Document Number
DGPU 1/5 (PEG)
Rev
F3A
Date: Wednesday, April 17, 2013
Sheet 16 of 46


U35B
[MEMORY I/F A]
[21] FBA_CMD[30:0]
[21] VMA_DM[7..0]
DBI
[21] VMA_WDQS[7..0]
EDC
[21] VMA_RDQS[7..0]
+1.5V_GFX
0816 follow DG to place caps
LAYOUT NOTES:
UNDAER: WITHIN 150MILS
NEAR: WITHIN 1378MILS
PLACE UNDER GPU BALLS
0.1u x 6 stuff x4
1u x 6 stuff x4
4.7u x 6 stuff x4
10u x 4 stuff x2
22u x 4 stuff x2
PLACE NEAR TO GPU BALLS
EV@N14P_GT
RSVD 330u, ZQS have one
15mils width
0815 no stuff follow CRB
GC6 connect to EC
EC_FB_CLAMP [19,20,34]
C6218 close ball K27 35mA
PLACE NEAR TO GPU BALLS
PLACE UNDER GPU BALLS
+FB_PLLAVDD = 0.3mm 12mils
U27+H17 62mA
Layout Notes: PLACE CLOSE TO GPU BALLS
0813
sDDR3
R1=42.2/F
R2=51.1/F
U35C
MEMORY I/F C
[22] FBC_CMD[30:0]
[22] VMC_DM[7..0]
[22] VMC_WDQS[7..0]
[22] VMC_RDQS[7..0]
0815 confirm with ZQS (sDDR3)
VMA_DQ[63:0] [21]
VMC_DQ[63:0] [22]
0815 no stuff follow CRB
1012(FAE)：Reserve +FB_PLLAVDD evan without CH-B
C107 close to ball H17
Quanta Computer Inc.
PROJECT : ZQK
Document Number
DGPU 2/5 (Memory)
Rev F3A
Date: Wednesday, April 17, 2013
Sheet 17 of 46



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PROJECT : ZQK

Size	Document Number	Rev
	DGPU 3/5 (Display)	F3A
Date: Wednesday, April 17, 2013	Sheet 18 of 46	

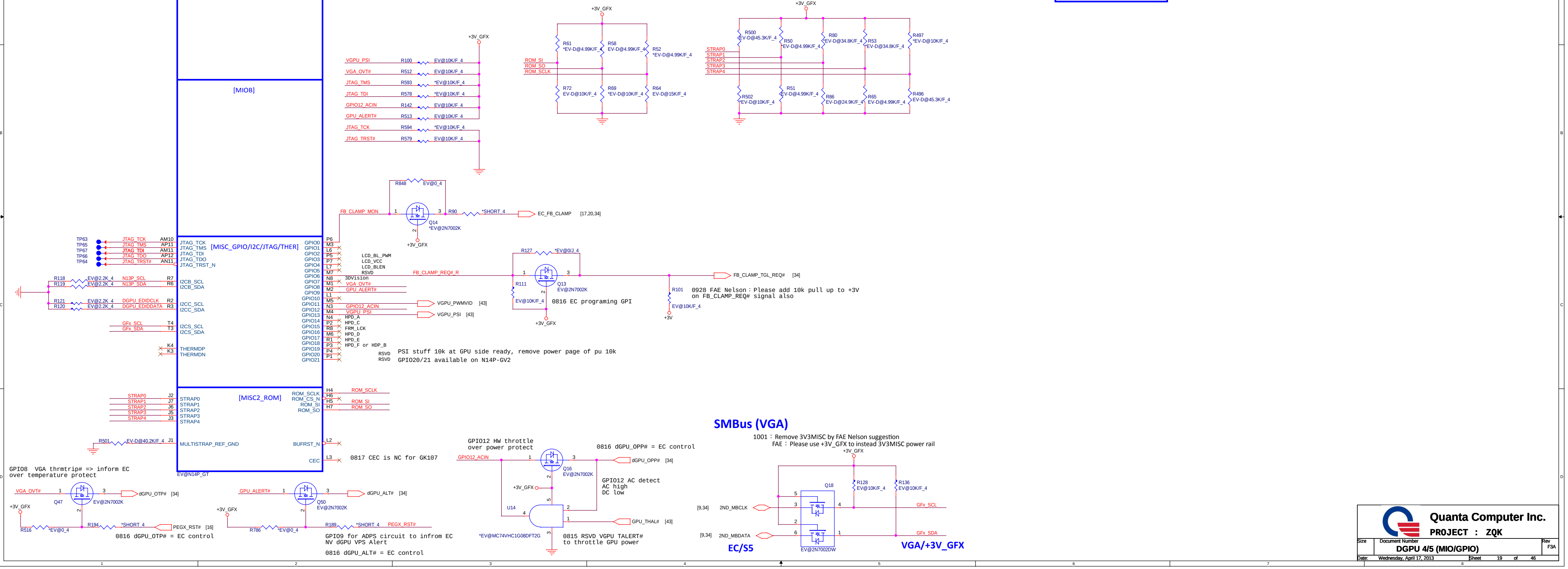
Logical Strap Bit Mapping

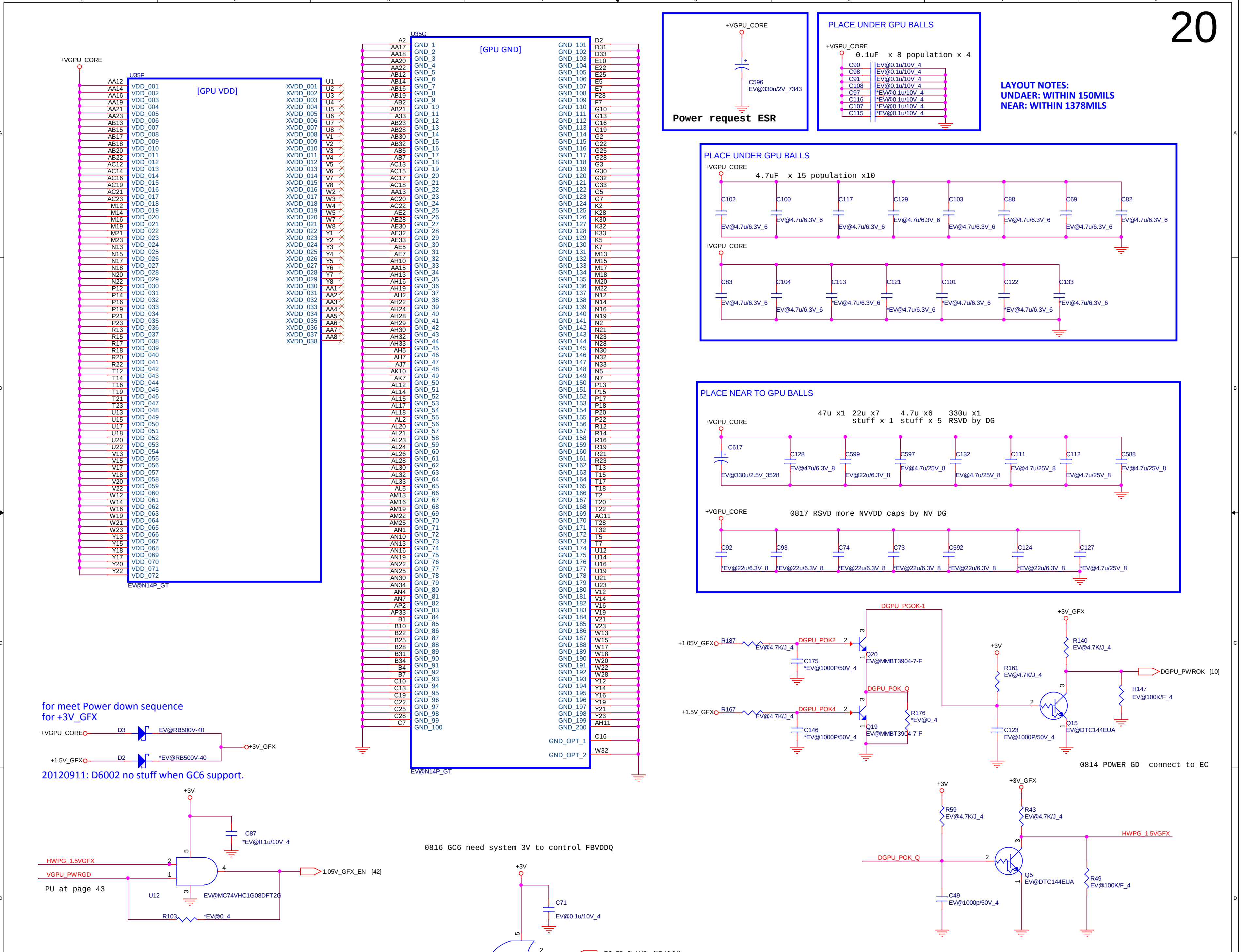
	PU-VDD	PD
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	FB_1	FB_0	SMB_ALT_ADDR	VGA_DEVICE	1000
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM	1292
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	0010
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0000
STRAP4	RESERVED	PCIE SPEED CHANGE GEN3	PCIE_MAX SPEED	DP_PLL_VDD33	0111

STRAP3
Optimus ---> 4.99k PD
Discrete only ---> 15K PD

Resistor P/N
4.99K---> CS24992FB26
10K ---> CS31002FB26
15K ---> CS31502FB24
20K ---> CS32002FB29
24.9K---> CS32492FB16
30.1K---> CS33012FB18
34.8K---> CS33482FB22
45.3K---> CS34532FB18





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PROJECT : ZQK

Size | Document Number: DGPU 5/5 (Power/Ground) | Rev F3A

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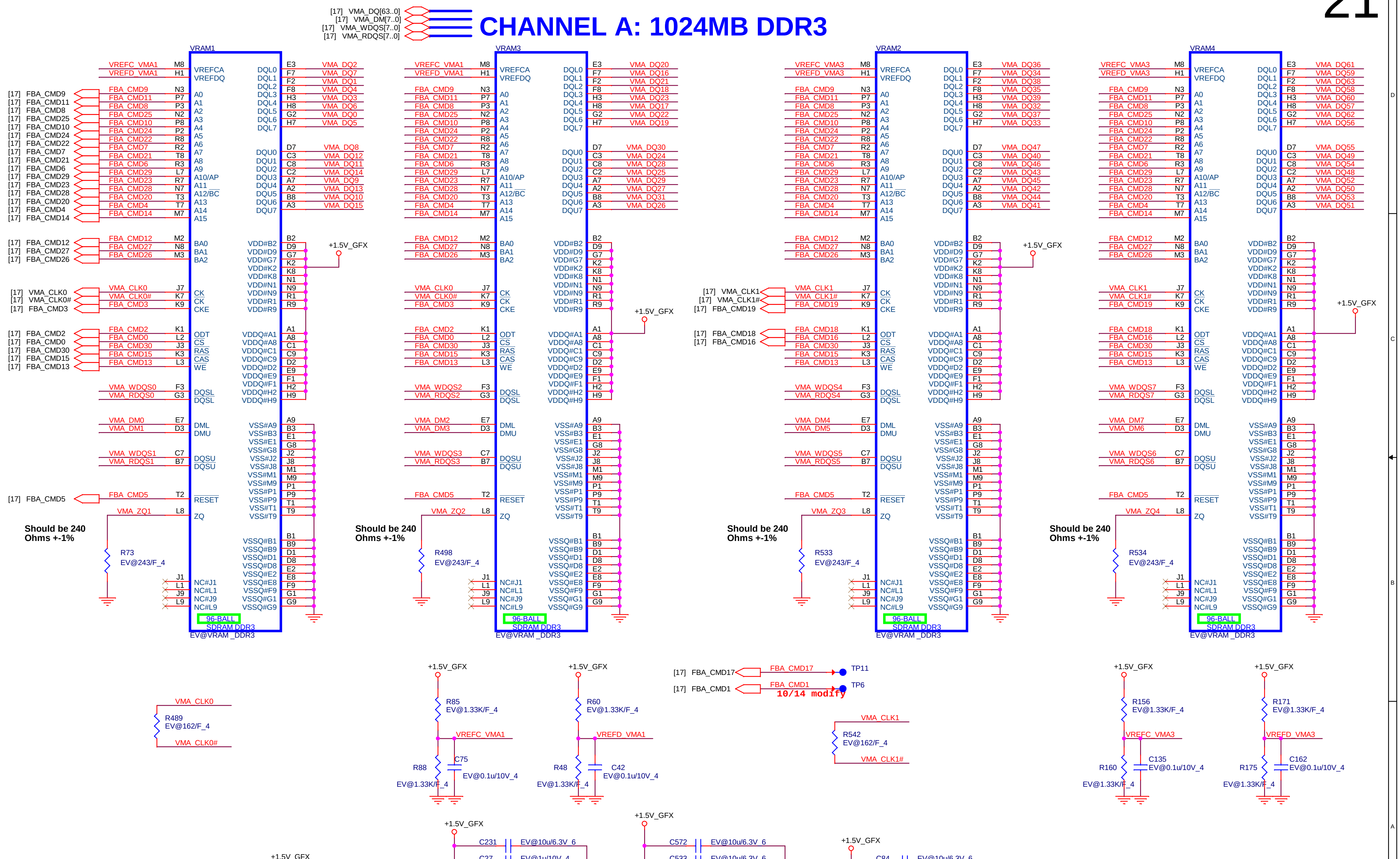
CHANNEL A: 1024MB DDR3



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PROJECT : ZQK

Size	Document Number	Rev
	NN13P-LP DDR3 VRAM 1/2	F3A

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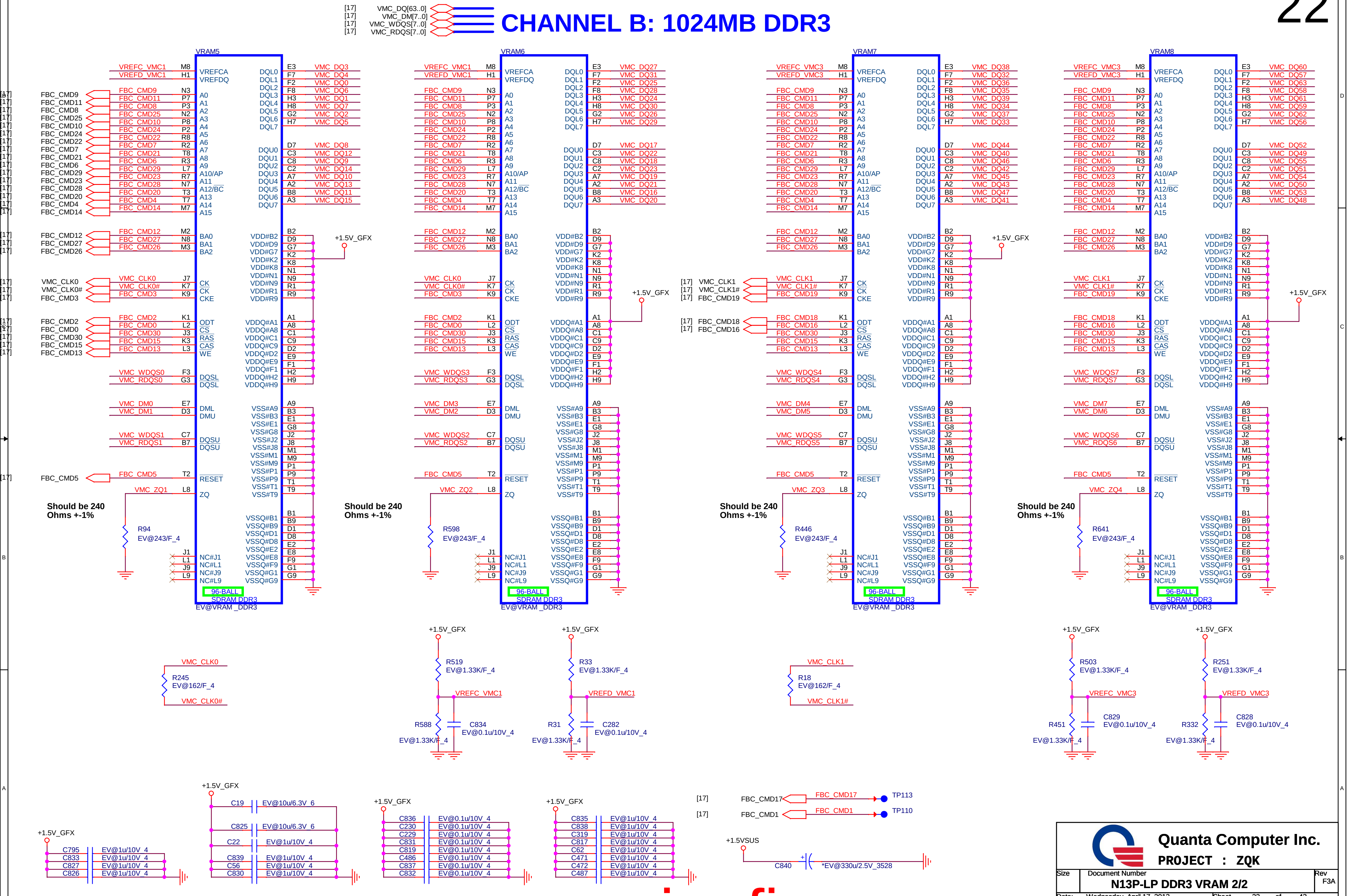
CHANNEL B: 1024MB DDR3



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PROJECT : ZQK

Size	Document Number	Rev
	N13P-LP DDR3 VRAM 2/2	F3A

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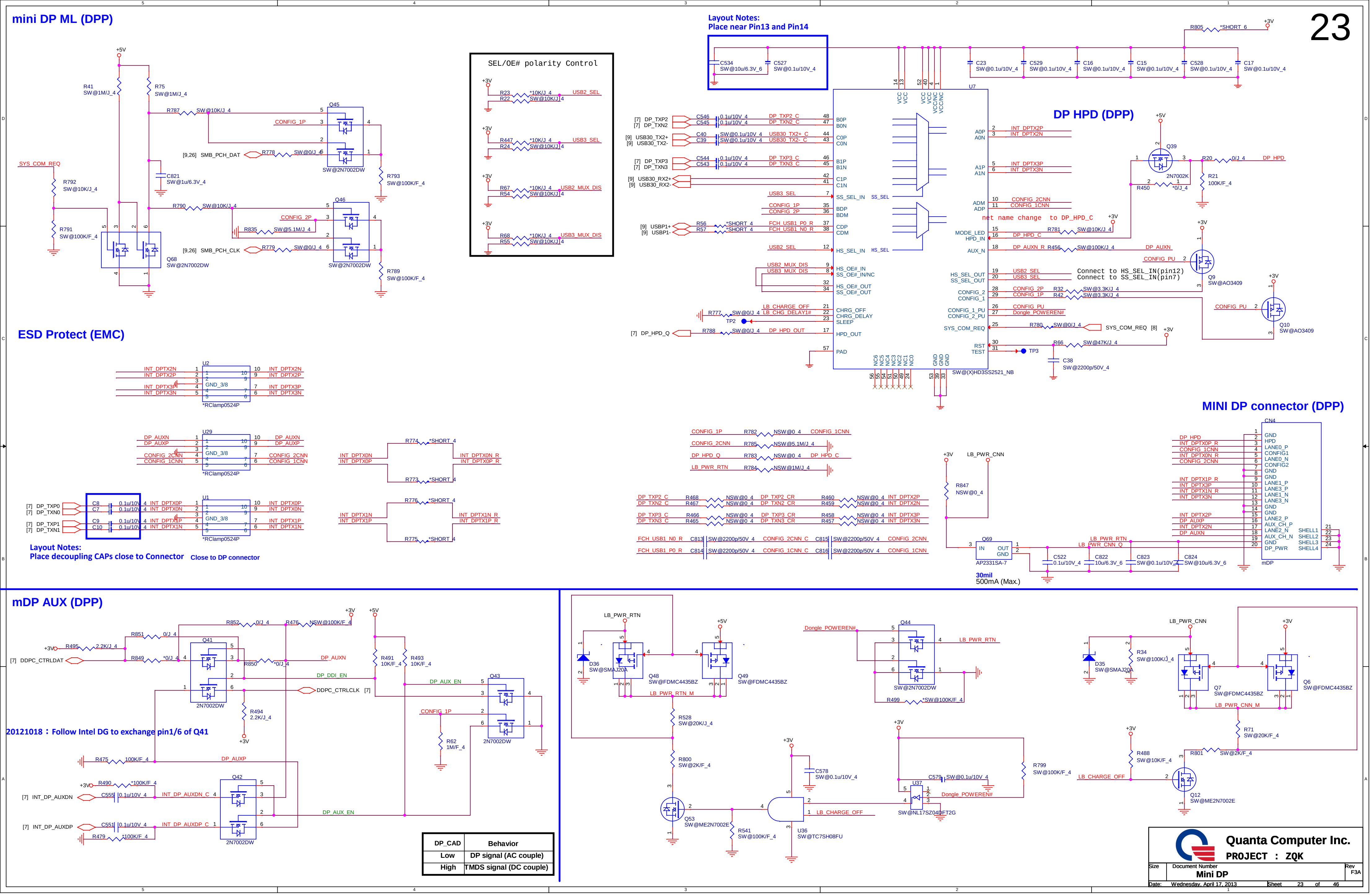
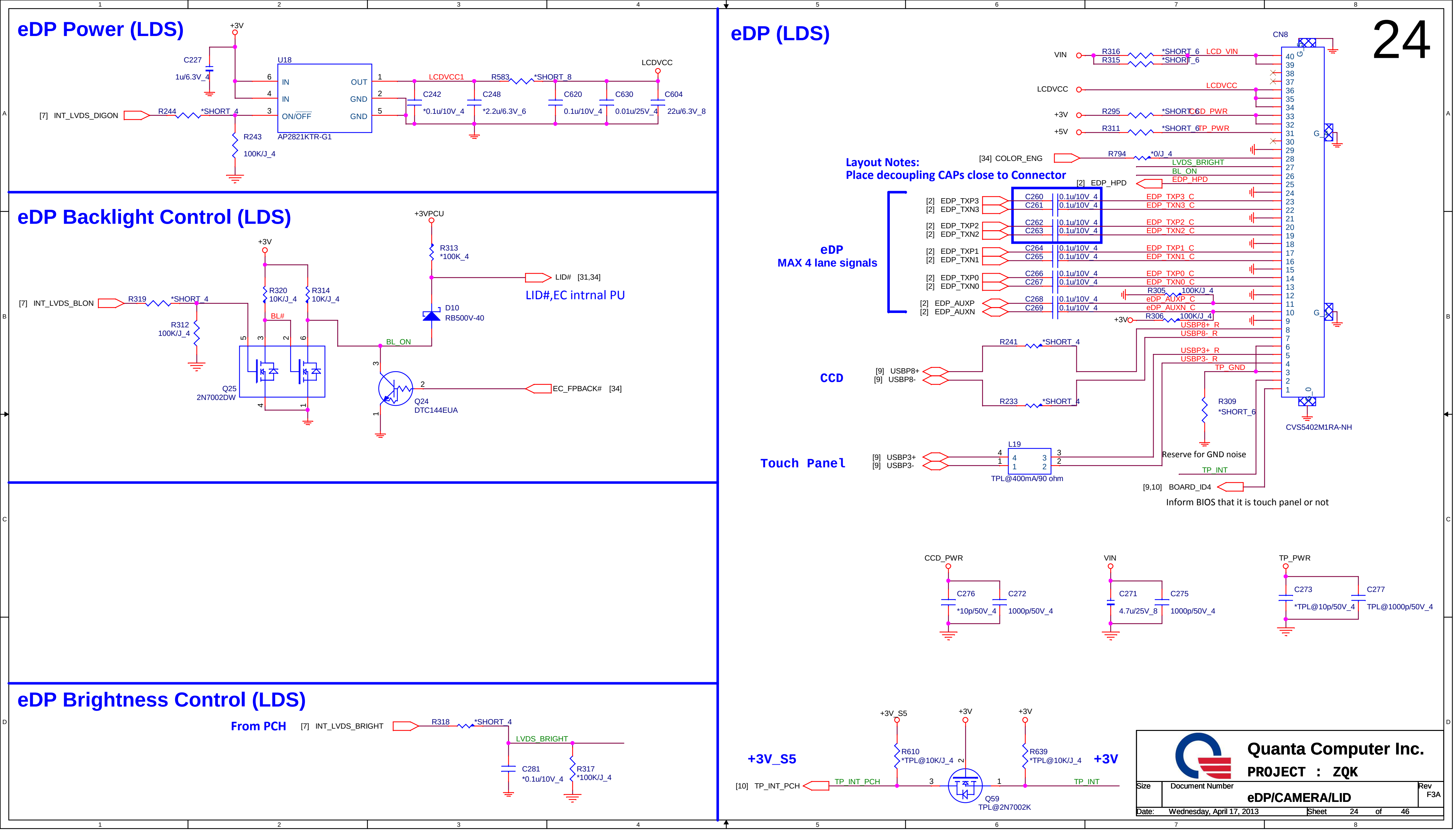


DP_CAD	Behavior
Low	DP signal (AC couple)
High	TMDS signal (DC couple)


24
eDP Power (LDS)
+3V
C227
1u/6.3V_4
U18
IN
IN
ON/OFF
OUT
GND
GND
AP2821KTR-G1
[7] INT_LVDS_DIGON
R244 *SHORT_4
R243
100K/J_4
LCDVCC1
R583 *SHORT_8
LCDVCC
C242 *0.1u/10V_4
C248 *2.2u/6.3V_6
C620 0.1u/10V_4
C630 0.01u/25V_4
C604 22u/6.3V_8
eDP Backlight Control (LDS)
+3VPCU
R313 *100K_4
LID# [31,34]
LID#,EC intrnal PU
D10 RB500V-40
+3V
R320 10K/J_4
R314 10K/J_4
BL#
[7] INT_LVDS_BLON
R319 *SHORT_4
R312 100K/J_4
Q25 2N7002DW
BL_ON
Q24 DTC144EUA
EC_FPBACK# [34]
eDP Brightness Control (LDS)
From PCH
[7] INT_LVDS_BRIGHT
R318 *SHORT_4
LVDS_BRIGHT
C281 *0.1u/10V_4
R317 *100K/J_4
eDP (LDS)
CN8
VIN
R316 *SHORT_6 LCD_VIN
R315 *SHORT_6
LCDVCC
+3V R295 *SHORT_6 CCD_PWR
+5V R311 *SHORT_6 TP_PWR
Layout Notes:
Place decoupling CAPs close to Connector
[34] COLOR_ENG R794 *0/J_4
LVDS_BRIGHT
BL_ON
[2] EDP_HPD
EDP_HPD
eDP
MAX 4 lane signals
[2] EDP_TXP3 C260 0.1u/10V_4 EDP_TXP3_C
[2] EDP_TXN3 C261 0.1u/10V_4 EDP_TXN3_C
[2] EDP_TXP2 C262 0.1u/10V_4 EDP_TXP2_C
[2] EDP_TXN2 C263 0.1u/10V_4 EDP_TXN2_C
[2] EDP_TXP1 C264 0.1u/10V_4 EDP_TXP1_C
[2] EDP_TXN1 C265 0.1u/10V_4 EDP_TXN1_C
[2] EDP_TXP0 C266 0.1u/10V_4 EDP_TXP0_C
[2] EDP_TXN0 C267 0.1u/10V_4 EDP_TXN0_C
[2] EDP_AUXP C268 0.1u/10V_4 eDP_AUXP_C
[2] EDP_AUXN C269 0.1u/10V_4 eDP_AUXN_C
R305 100K/J_4
+3V R306 100K/J_4
USBP8+_R
USBP8-_R
CCD
[9] USBP8+
[9] USBP8-
R241 *SHORT_4
R233 *SHORT_4
USBP3+_R
USBP3-_R
TP_GND
R309 *SHORT_6
Reserve for GND noise
CVS5402M1RA-NH
Touch Panel
[9] USBP3+
[9] USBP3-
L19
TPL@400mA/90 ohm
TP_INT
[9,10] BOARD_ID4
Inform BIOS that it is touch panel or not
CCD_PWR
C276 *10p/50V_4
C272 1000p/50V_4
VIN
C271 4.7u/25V_8
C275 1000p/50V_4
TP_PWR
C273 *TPL@10p/50V_4
C277 TPL@1000p/50V_4
+3V_S5
+3V
R610 *TPL@10K/J_4
R639 *TPL@10K/J_4
[10] TP_INT_PCH
TP_INT_PCH
TP_INT
Q59 TPL@2N7002K
Quanta Computer Inc.
PROJECT : ZQK
Size
Document Number
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F3A
eDP/CAMERA/LID
Date: Wednesday, April 17, 2013
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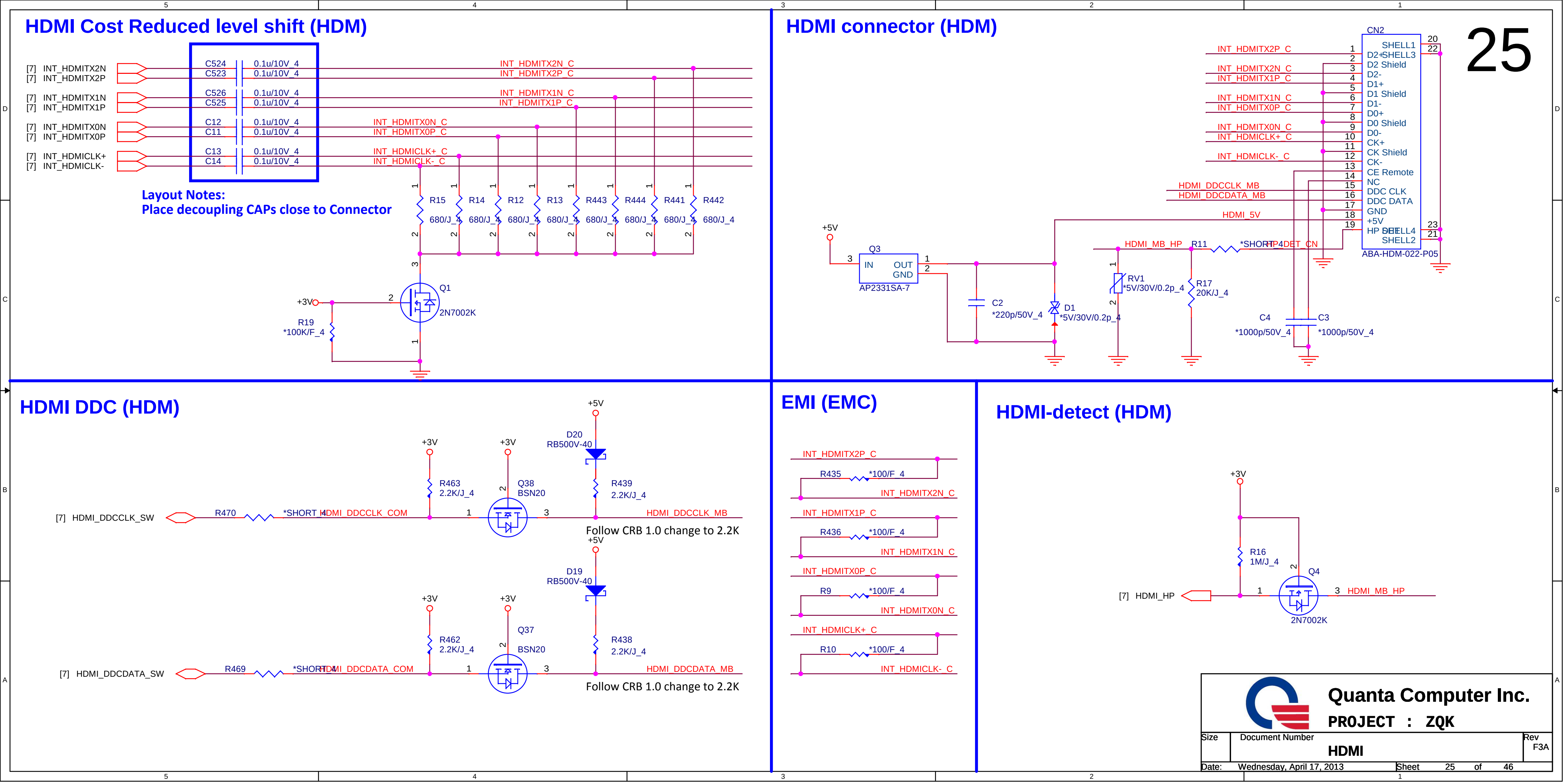
25
HDMI Cost Reduced level shift (HDM)
[7] INT_HDMITX2N
[7] INT_HDMITX2P
[7] INT_HDMITX1N
[7] INT_HDMITX1P
[7] INT_HDMITX0N
[7] INT_HDMITX0P
[7] INT_HDMICLK+
[7] INT_HDMICLK-
C524 0.1u/10V_4
C523 0.1u/10V_4
C526 0.1u/10V_4
C525 0.1u/10V_4
C12 0.1u/10V_4
C11 0.1u/10V_4
C13 0.1u/10V_4
C14 0.1u/10V_4
INT_HDMITX2N_C
INT_HDMITX2P_C
INT_HDMITX1N_C
INT_HDMITX1P_C
INT_HDMITX0N_C
INT_HDMITX0P_C
INT_HDMICLK+_C
INT_HDMICLK-_C
Layout Notes:
Place decoupling CAPs close to Connector
R15 680/J_4
R14 680/J_4
R12 680/J_4
R13 680/J_4
R443 680/J_4
R444 680/J_4
R441 680/J_4
R442 680/J_4
+3V
R19
*100K/F_4
Q1
2N7002K
HDMI connector (HDM)
CN2
SHELL1
D2+SHELL3
D2 Shield
D2-
D1+
D1 Shield
D1-
D0+
D0 Shield
D0-
CK+
CK Shield
CK-
CE Remote
NC
DDC CLK
DDC DATA
GND
+5V
HP DET
SHELL4
SHELL2
ABA-HDM-022-P05
HDMI_DDCCLK_MB
HDMI_DDCDATA_MB
HDMI_5V
HDMI_MB_HP
R11
*SHORT_4
HP_DET_CN
+5V
Q3
IN
OUT
GND
AP2331SA-7
C2
*220p/50V_4
D1
*5V/30V/0.2p_4
RV1
*5V/30V/0.2p_4
R17
20K/J_4
C4
*1000p/50V_4
C3
*1000p/50V_4
HDMI DDC (HDM)
[7] HDMI_DDCCLK_SW
R470
*SHORT_4
HDMI_DDCCLK_COM
+3V
R463
2.2K/J_4
Q38
BSN20
+5V
D20
RB500V-40
R439
2.2K/J_4
HDMI_DDCCLK_MB
Follow CRB 1.0 change to 2.2K
[7] HDMI_DDCDATA_SW
R469
*SHORT_4
HDMI_DDCDATA_COM
R462
2.2K/J_4
Q37
BSN20
D19
RB500V-40
R438
2.2K/J_4
HDMI_DDCDATA_MB
Follow CRB 1.0 change to 2.2K
EMI (EMC)
INT_HDMITX2P_C
R435 *100/F_4
INT_HDMITX2N_C
INT_HDMITX1P_C
R436 *100/F_4
INT_HDMITX1N_C
INT_HDMITX0P_C
R9 *100/F_4
INT_HDMITX0N_C
INT_HDMICLK+_C
R10 *100/F_4
INT_HDMICLK-_C
HDMI-detect (HDM)
+3V
R16
1M/J_4
Q4
2N7002K
[7] HDMI_HP
HDMI_MB_HP
Quanta Computer Inc.
PROJECT : ZQK
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HDMI
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F3A
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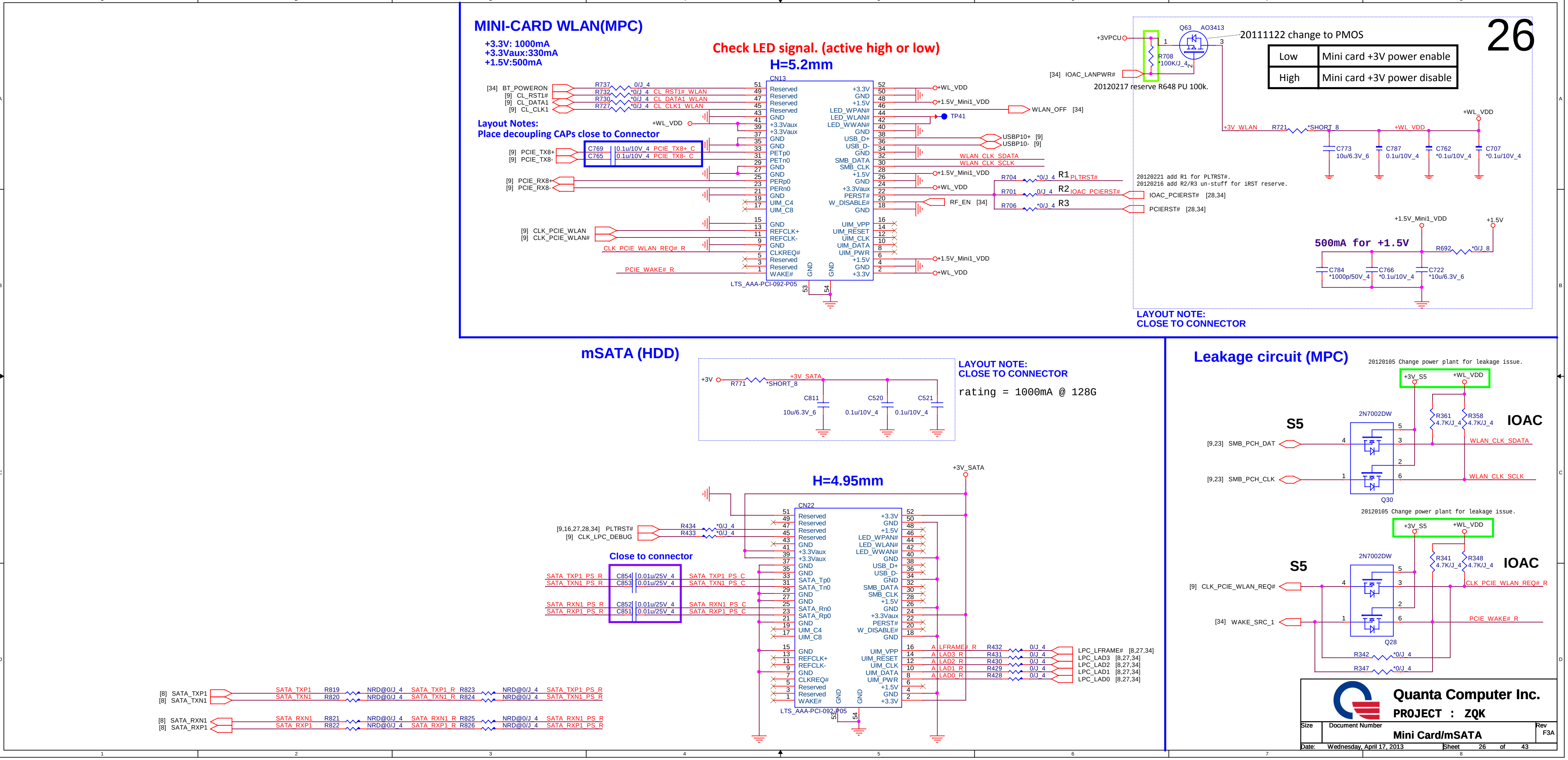
26
MINI-CARD WLAN(MPC)
+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA
Check LED signal. (active high or low)
H=5.2mm
Layout Notes:
Place decoupling CAPs close to Connector
LTS_AAA-PCI-092-P05
20111122 change to PMOS
Low
Mini card +3V power enable
High
Mini card +3V power disable
20120217 reserve R648 PU 100k.
20120221 add R1 for PLTRST#.
20120216 add R2/R3 un-stuff for iRST reserve.
500mA for +1.5V
LAYOUT NOTE:
CLOSE TO CONNECTOR
mSATA (HDD)
LAYOUT NOTE:
CLOSE TO CONNECTOR
rating = 1000mA @ 128G
H=4.95mm
Close to connector
Leakage circuit (MPC)
20120105 Change power plant for leakage issue.
S5
IOAC
2N7002DW
Q30
Q28
Quanta Computer Inc.
PROJECT : ZQK
Mini Card/mSATA
Rev F3A
Date: Wednesday, April 17, 2013
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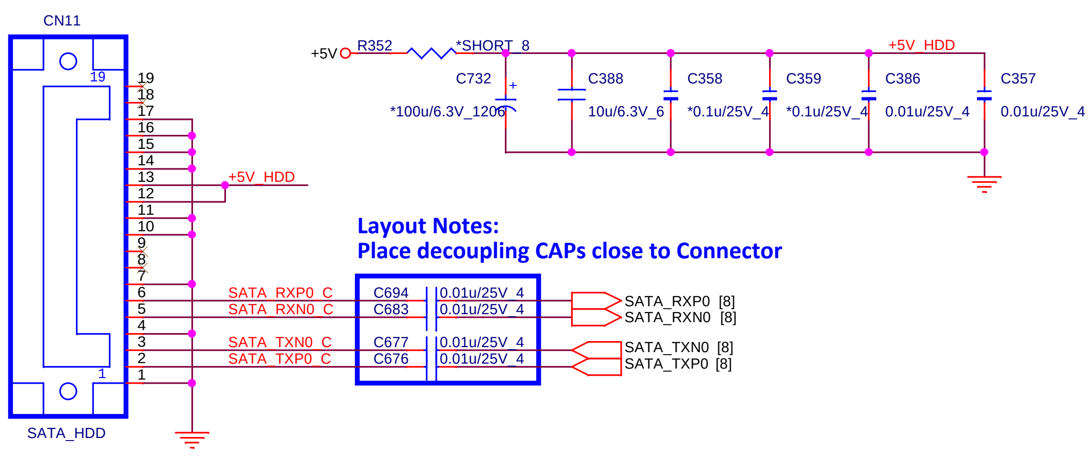
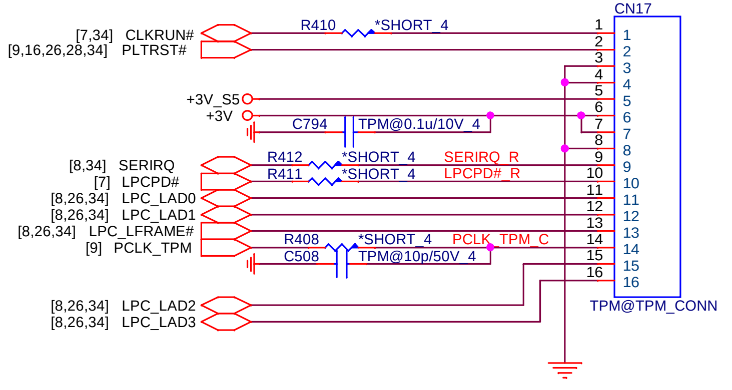
MAIN SATA HDD (HDD)

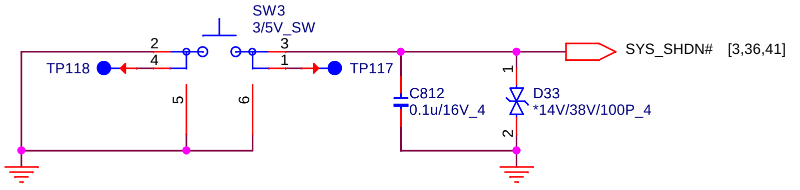


Layout Notes:
Place decoupling CAPs close to Connector

TPM (TPM)



3/5VPCU reset switch (CLG)



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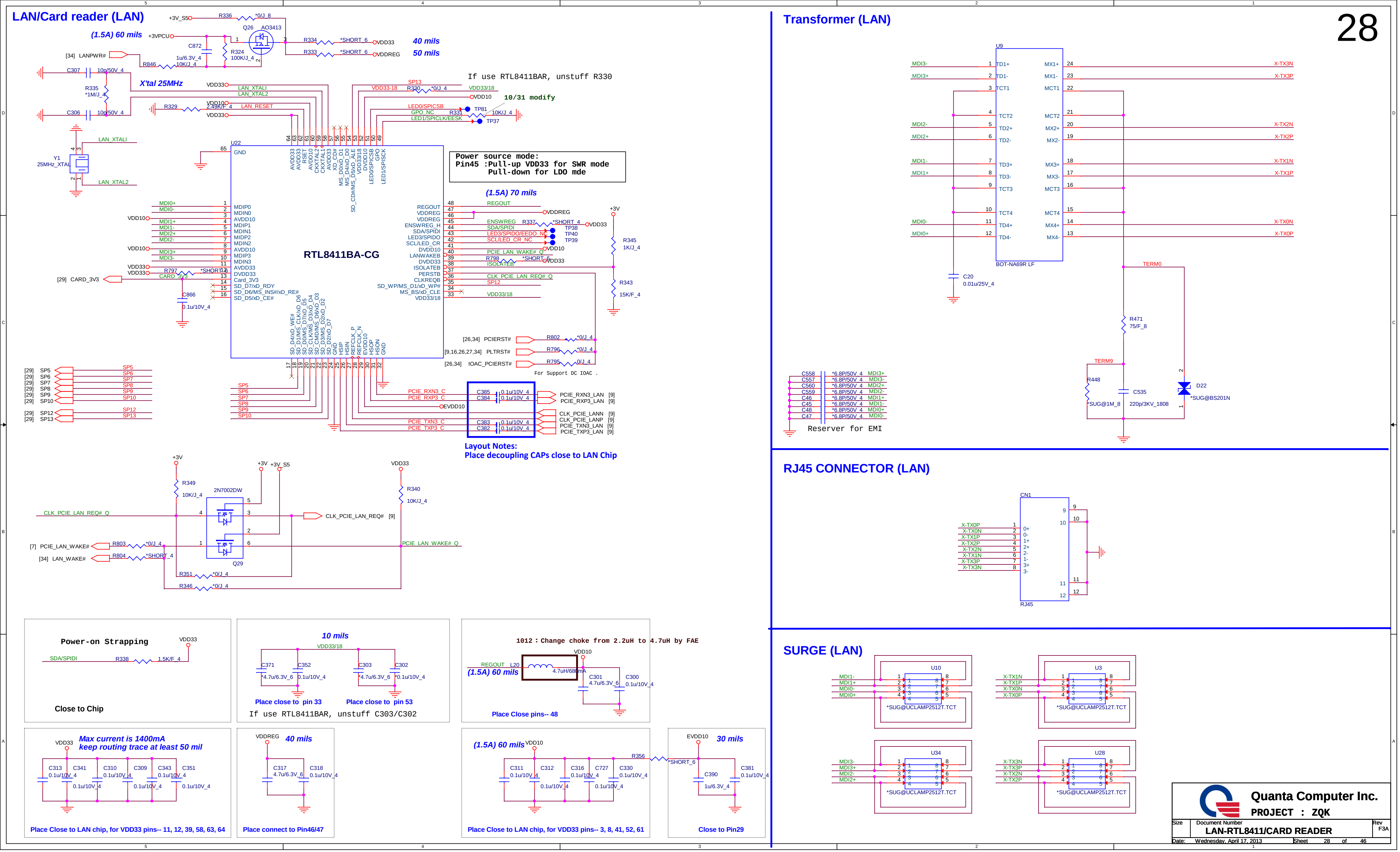
PROJECT : ZQK

Size	Document Number	Rev
	SATA-HDD/ TPM	F3A

Date: Wednesday, April 17, 2013 Sheet 27 of 46


LAN/Card reader (LAN)
28
Transformer (LAN)
(1.5A) 60 mils
40 mils
50 mils
X'tal 25MHz
If use RTL8411BAR, unstuff R330
10/31 modify
Power source mode:
Pin45 :Pull-up VDD33 for SWR mode
Pull-down for LDO mde
(1.5A) 70 mils
RTL8411BA-CG
For Support DC IOAC .
Layout Notes:
Place decoupling CAPs close to LAN Chip
BOT-NA69R LF
Reserver for EMI
RJ45 CONNECTOR (LAN)
SURGE (LAN)
Power-on Strapping
Close to Chip
10 mils
Place close to pin 33
Place close to pin 53
If use RTL8411BAR, unstuff C303/C302
1012 : Change choke from 2.2uH to 4.7uH by FAE
Place Close pins-- 48
Max current is 1400mA
keep routing trace at least 50 mil
Place Close to LAN chip, for VDD33 pins-- 11, 12, 39, 58, 63, 64
Place connect to Pin46/47
30 mils
Place Close to LAN chip, for VDD33 pins-- 3, 8, 41, 52, 61
Close to Pin29
Quanta Computer Inc.
PROJECT : ZQK
Size
Document Number
LAN-RTL8411/CARD READER
Rev
F3A
Date: Wednesday, April 17, 2013
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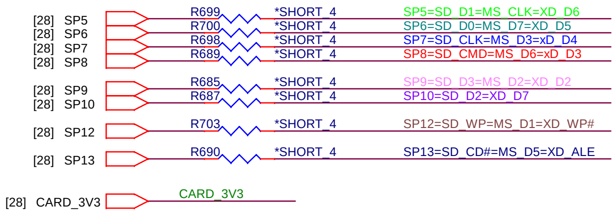
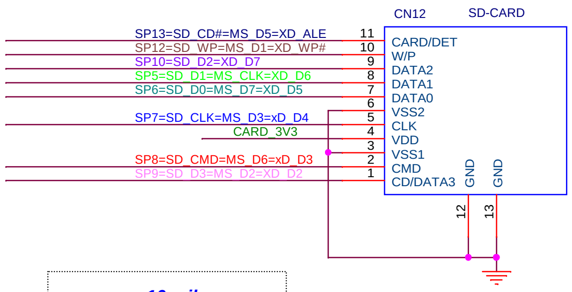
CARD READER CONNECTOR (MMC)

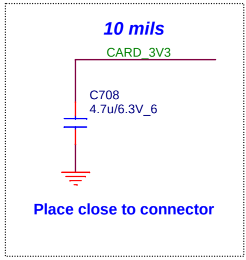
SD/MMC CARD READER (MMC)

Share Pin

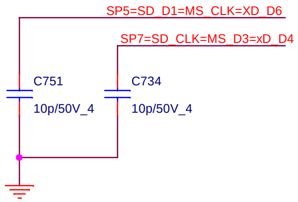
SP1	SD_D7		xD_RDY
SP2	SD_D6	MS_INS#	xD_RE#
SP3	SD_D5		xD_CE#
SP4	SD_D4		xD_WE#
SP5	SD_D1	MS_CLK	xD_D6
SP6	SD_D0	MS_D7	xD_D5
SP7	SD_CLK	MS_D3	xD_D4
SP8	SD_CMD	MS_D6	xD_D3
SP9	SD_D3	MS_D2	xD_D2
SP10	SD_D2		xD_D7
SP11		MS_BS	xD_CLE
SP12	SD_WP	MS_D1	xD_WP#
SP13	SD_CD#	MS_D5	xD_ALE
SP14		MS_D4	xD_D0
SP15		MS_D0	xD_D1
SP16			xD_CD#







EMI



Quanta Computer Inc.

PROJECT : ZQK

Size	Document Number	Rev
	CARD READER CONNECTOR	F3A
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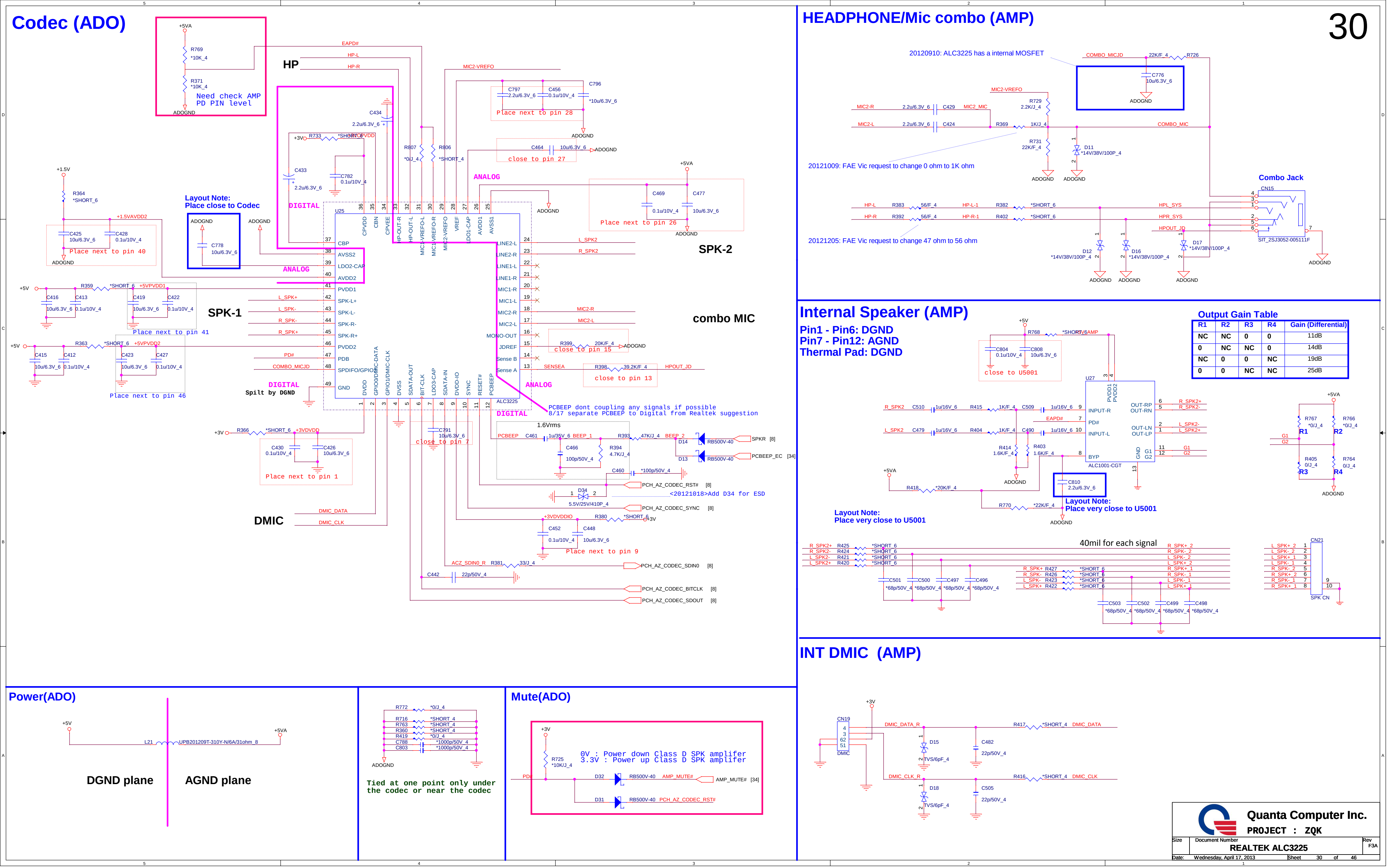
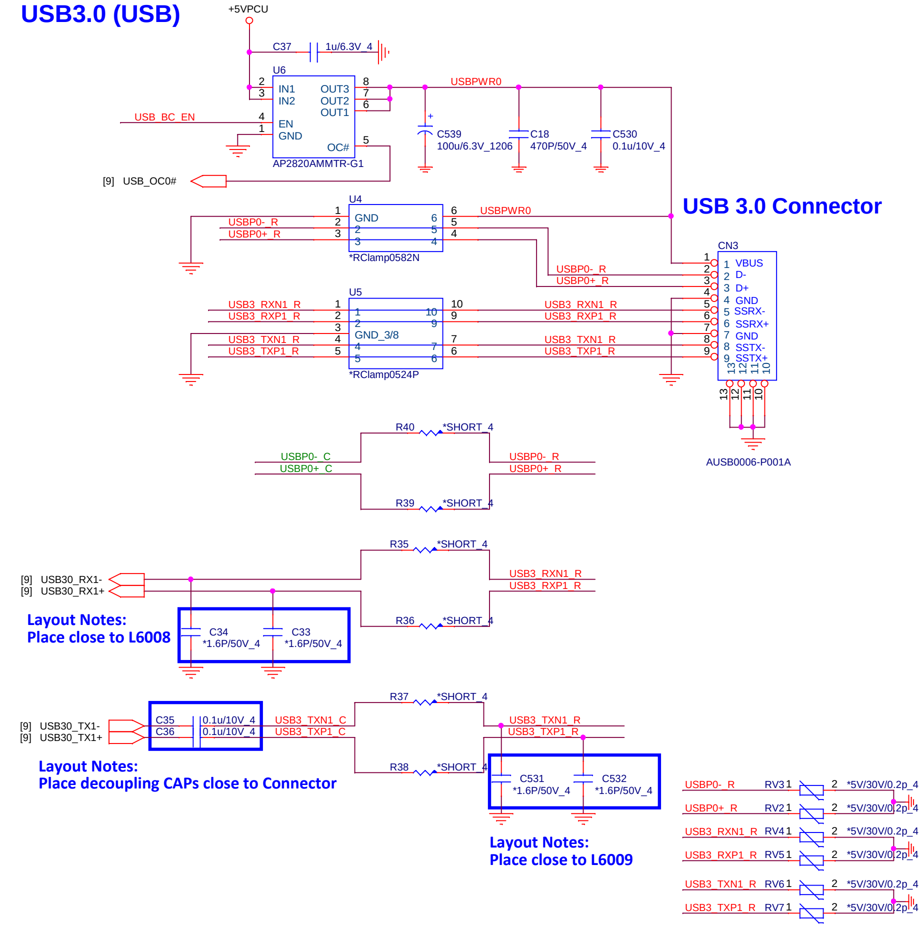


Output Gain Table

R1	R2	R3	R4	Gain (Differential)
NC	NC	0	0	11dB
0	NC	NC	0	14dB
NC	0	0	NC	19dB
0	0	NC	NC	25dB

USB3.0 (USB)

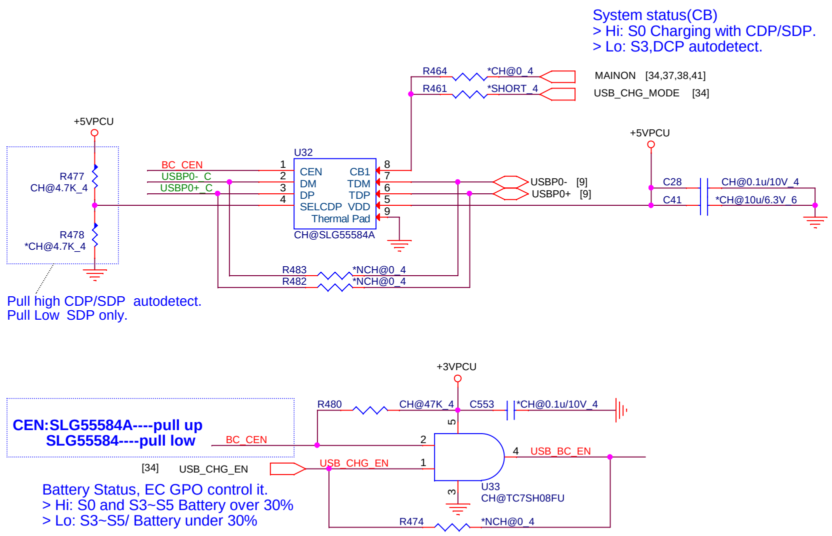


USB Charger to 3.0 (USB)

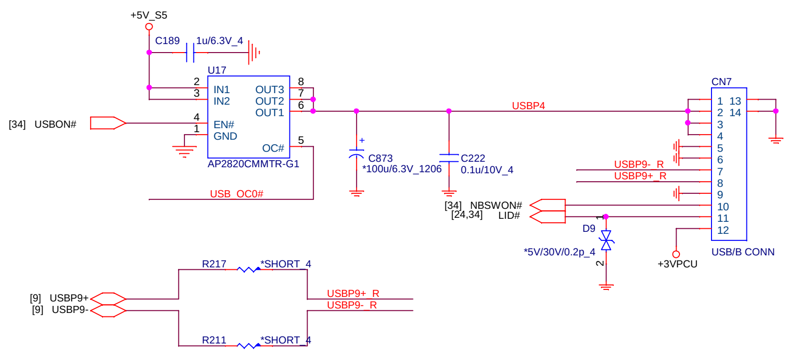
Name	USB data	State	Max Current	Apple Device
SDP	YES	S0~S3	500mA	500mA
CDP	YES	S0~S3	1500mA	500mA
DCP,Auto	NO	S4~S5	1800mA	1800mA

CB	SELCDP	FuncionFuncion
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only (depending on external device)

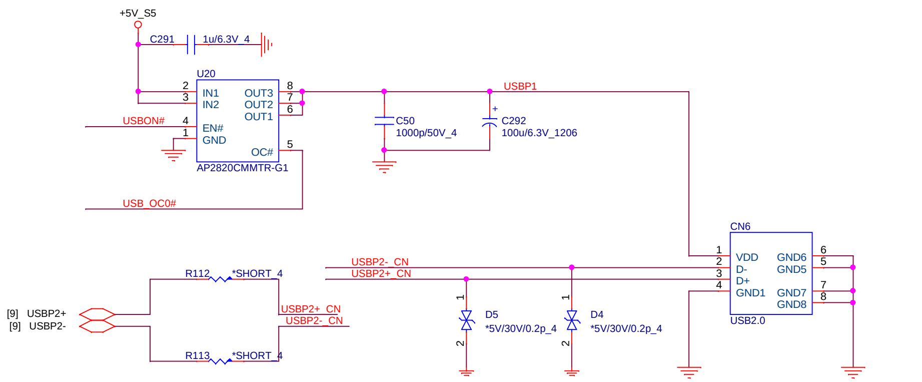
CH@: Default stuff



I/O board (USB)



USB2.0 (USB)



Quanta Computer Inc.
PROJECT : ZQK
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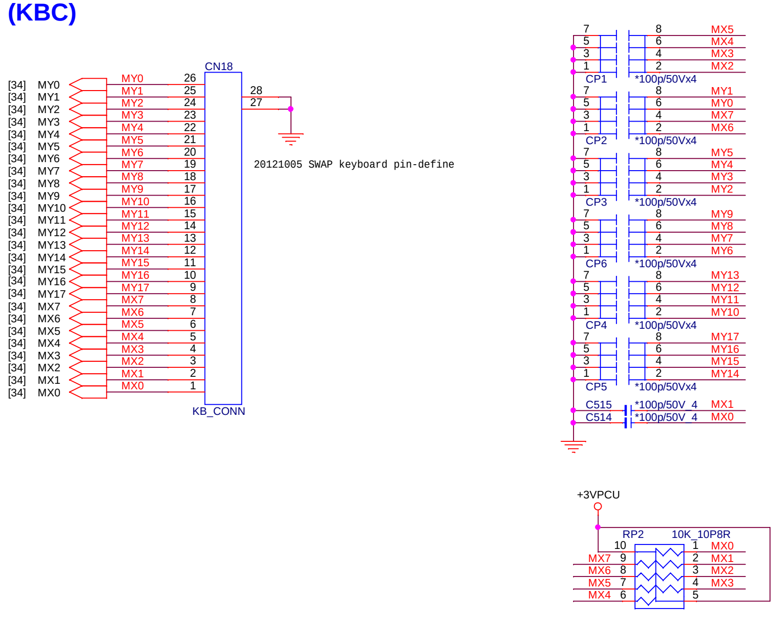
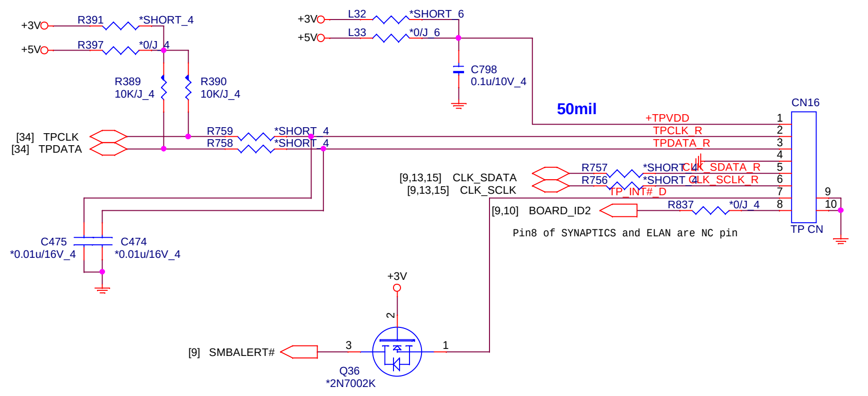
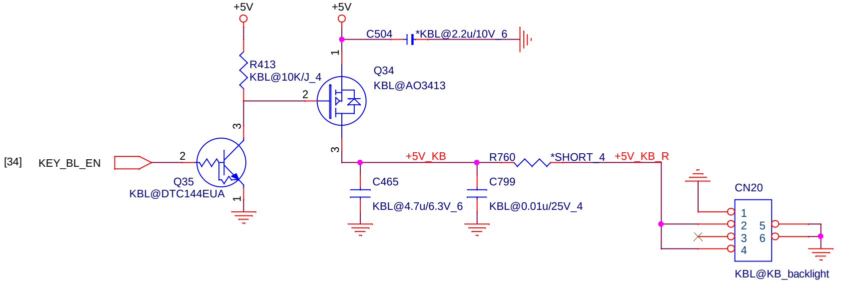
K/B (KBC)



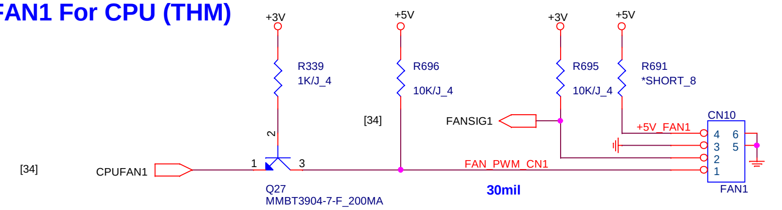
TOUCHPAD BOARD CONN (TPD)



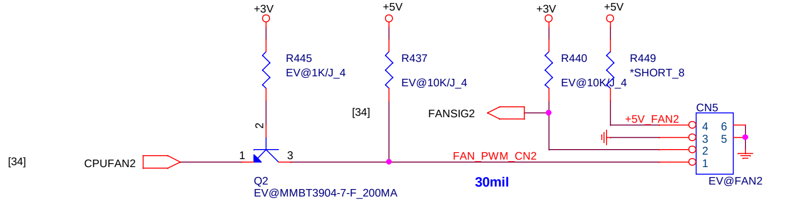
KB_BL LED (KBC)



FAN1 For CPU (THM)



FAN2 For GPU (THM)



Quanta Computer Inc.

PROJECT : ZQK

Size	Document Number	Rev
	KB/TP/FAN	F3A

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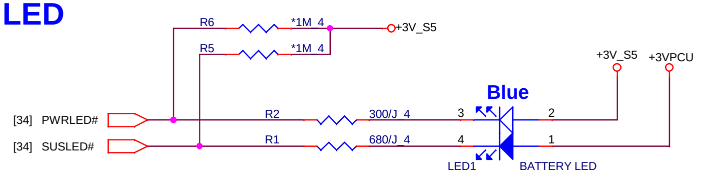
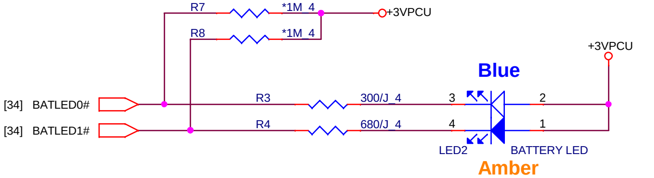
LED(UIF)

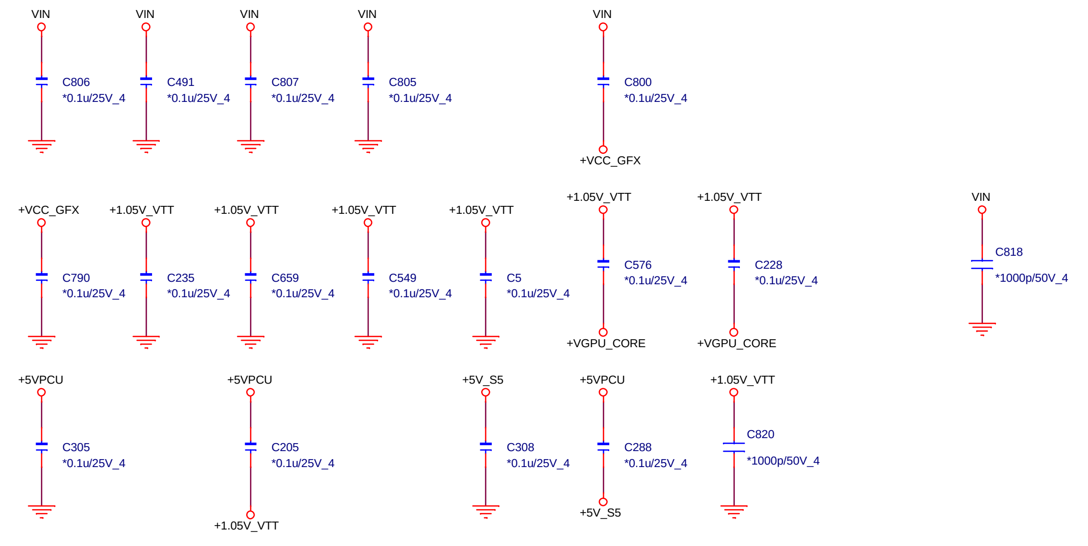
Power LED



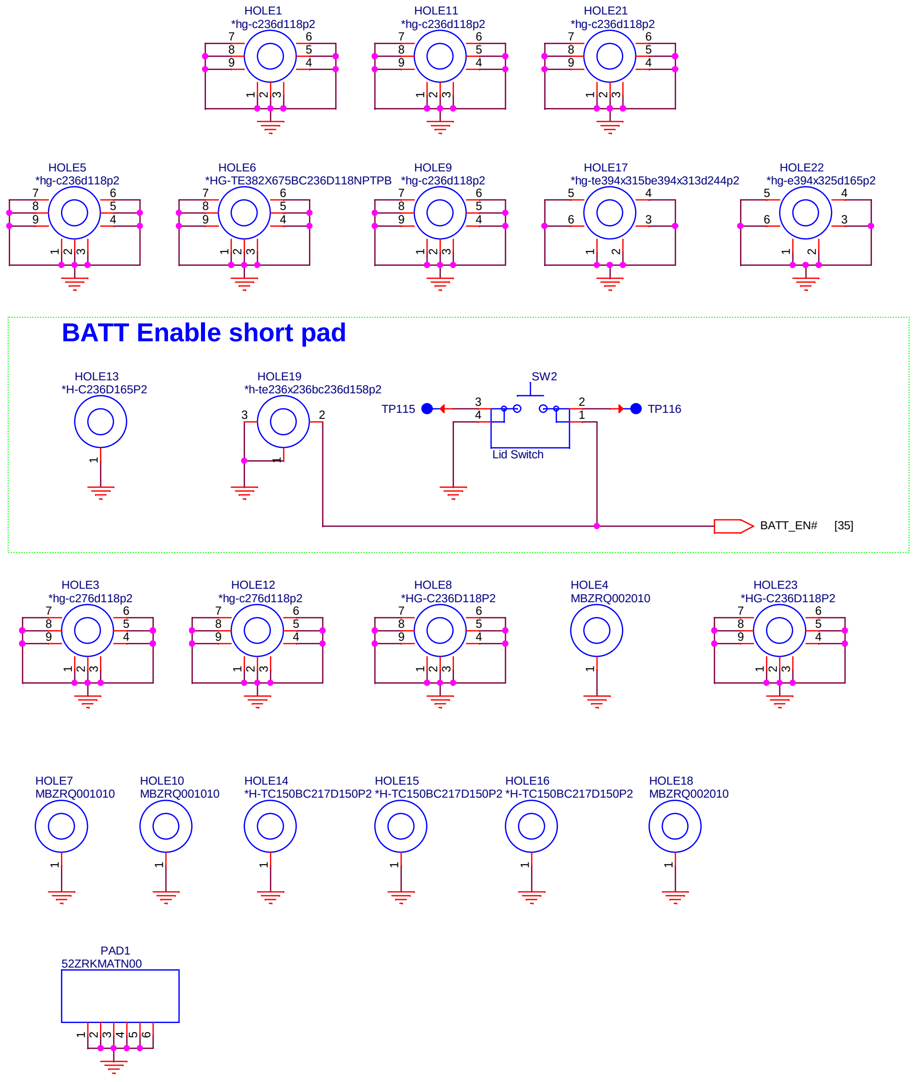
Battery



Stitching cap (EMC)



HOLE(OTH)



Quanta Computer Inc.		
PROJECT : ZQK		
Size	Document Number: LED/ Hole	Rev F3A
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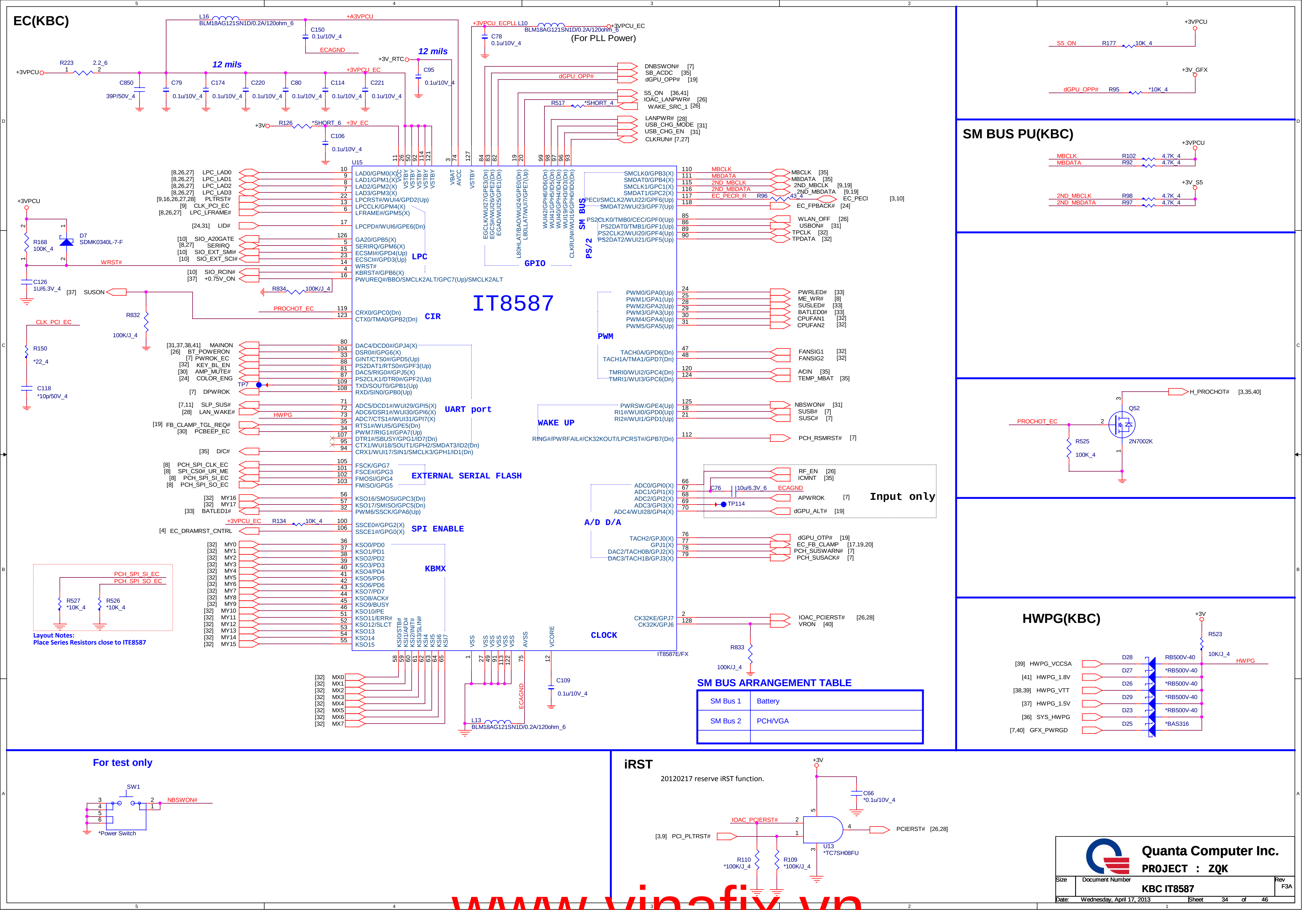

EC(KBC)
+3VPCU
+A3VPCU
L16
BLM18AG121SN1D/0.2A/120ohm_6
C150
0.1u/10V_4
ECAGND
12 mils
+3V_RTC
+3VPCU_EC
+3VPCU_ECPLL
L10
BLM18AG121SN1D/0.2A/120ohm_6
+3VPCU_EC
C78
0.1u/10V_4
(For PLL Power)
R223
2.2_6
C850
39P/50V_4
C79
C174
C220
C80
C114
C221
C95
0.1u/10V_4
R126
*SHORT_6
+3V_EC
C106
0.1u/10V_4
U15
IT8587
IT8587E/FX
LPC
GPIO
SM BUS
PS/2
CIR
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
SPI ENABLE
KBMX
A/D D/A
CLOCK
Input only
DNBSWON#
SB_ACDC
dGPU_OPP#
S5_ON
IOAC_LANPWR#
WAKE_SRC_1
LANPWR#
USB_CHG_MODE
USB_CHG_EN
CLKRUN#
R517
*SHORT_4
LPC_LAD0
LPC_LAD1
LPC_LAD2
LPC_LAD3
PLTRST#
CLK_PCI_EC
LPC_LFRAME#
LID#
SIO_A20GATE
SERIRQ
SIO_EXT_SMI#
SIO_EXT_SCI#
WRST#
SIO_RCIN#
+0.75V_ON
SUSON
R834
100K/J_4
PROCHOT_EC
R832
100K/J_4
D7
SDMK0340L-7-F
R168
100K_4
C126
1U/6.3V_4
CLK_PCI_EC
R150
*22_4
C118
*10p/50V_4
MAINON
BT_POWERON
PWROK_EC
KEY_BL_EN
AMP_MUTE#
COLOR_ENG
TP7
DPWROK
SLP_SUS#
LAN_WAKE#
HWPG
FB_CLAMP_TGL_REQ#
PCBEEP_EC
D/C#
PCH_SPI_CLK_EC
SPI_CS0#_UR_ME
PCH_SPI_SI_EC
PCH_SPI_SO_EC
MY16
MY17
BATLED1#
R134
10K_4
EC_DRAMRST_CNTRL
MY0 … MY15
MX0 … MX7
R527
*10K_4
R526
*10K_4
Layout Notes:
Place Series Resistors close to ITE8587
MBCLK
MBDATA
2ND_MBCLK
2ND_MBDATA
EC_PECI
R96
43_4
EC_FPBACK#
WLAN_OFF
USBON#
TPCLK
TPDATA
PWRLED#
ME_WR#
SUSLED#
BATLED0#
CPUFAN1
CPUFAN2
FANSIG1
FANSIG2
ACIN
TEMP_MBAT
NBSWON#
SUSB#
SUSC#
PCH_RSMRST#
RF_EN
ICMNT
C76
10u/6.3V_6
ECAGND
APWROK
TP114
dGPU_ALT#
dGPU_OTP#
EC_FB_CLAMP
PCH_SUSWARN#
PCH_SUSACK#
IOAC_PCIERST#
VRON
R833
100K/J_4
C109
0.1u/10V_4
L13
BLM18AG121SN1D/0.2A/120ohm_6
SM BUS ARRANGEMENT TABLE
SM Bus 1 Battery
SM Bus 2 PCH/VGA
R177
10K_4
+3V_GFX
R95
*10K_4
SM BUS PU(KBC)
R102
R92
4.7K_4
+3V_S5
R98
R97
H_PROCHOT#
Q52
2N7002K
R525
100K_4
HWPG(KBC)
+3V
R523
10K/J_4
HWPG_VCCSA
HWPG_1.8V
HWPG_VTT
HWPG_1.5V
SYS_HWPG
GFX_PWRGD
D28
D27
D26
D29
D23
D25
RB500V-40
*RB500V-40
*BAS316
For test only
SW1
*Power Switch
iRST
20120217 reserve iRST function.
C66
*0.1u/10V_4
PCI_PLTRST#
R110
*100K/J_4
R109
*100K/J_4
U13
*TC7SH08FU
PCIERST#
Quanta Computer Inc.
PROJECT : ZQK
Size
Document Number
Rev
KBC IT8587
F3A
Date: Wednesday, April 17, 2013
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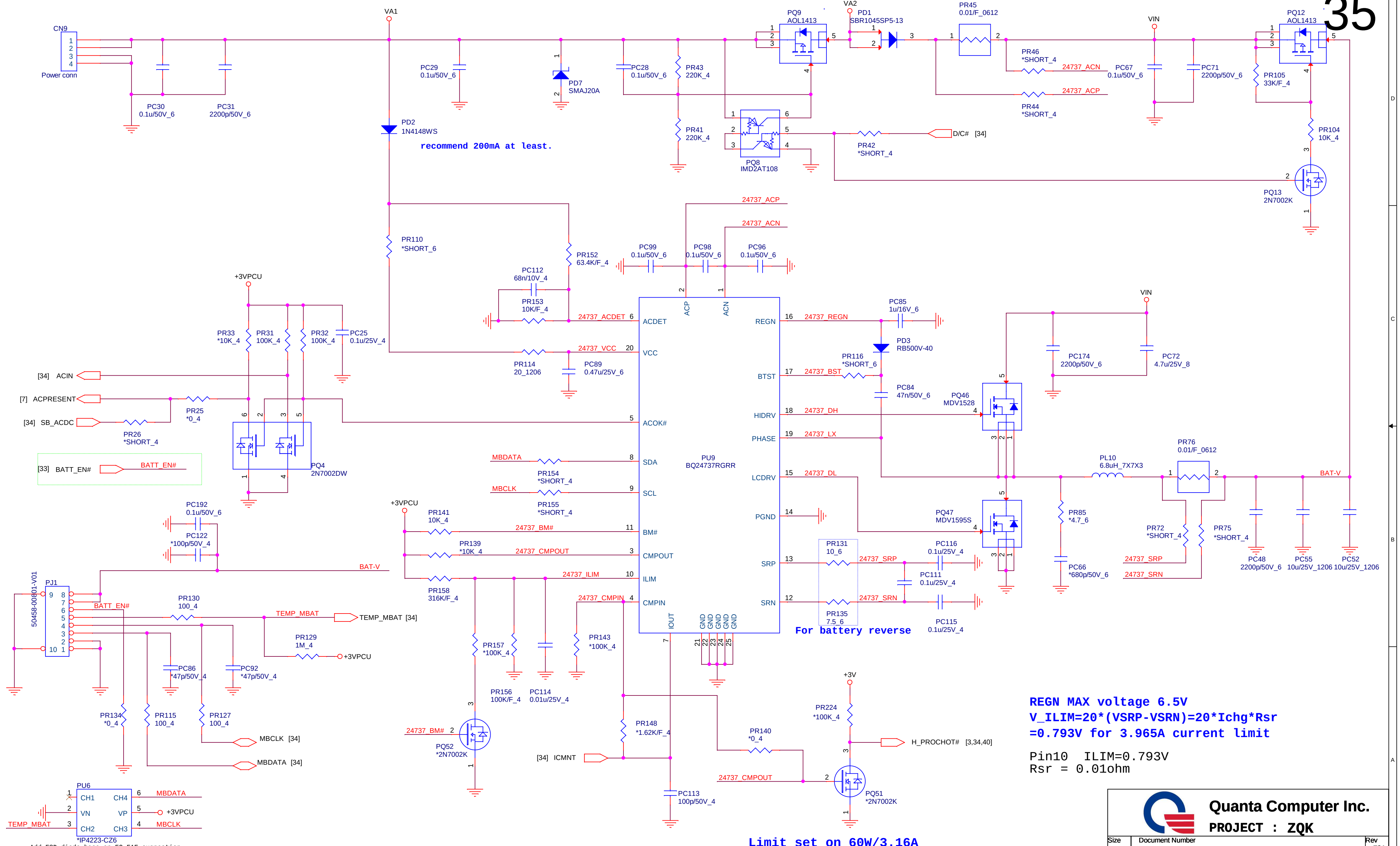

recommend 200mA at least.

For battery reverse

REGN MAX voltage 6.5V
V_ILIM=20*(VSRP-VSRN)=20*Ichg*Rsr
=0.793V for 3.965A current limit

Pin10 ILIM=0.793V
Rsr = 0.01ohm

Limit set on 60W/3.16A

Add ESD diode base on EC FAE suggestion

Quanta Computer Inc.
PROJECT : ZQK

Size	Document Number	Rev
	Charger(BQ24737RGRR)	F3A

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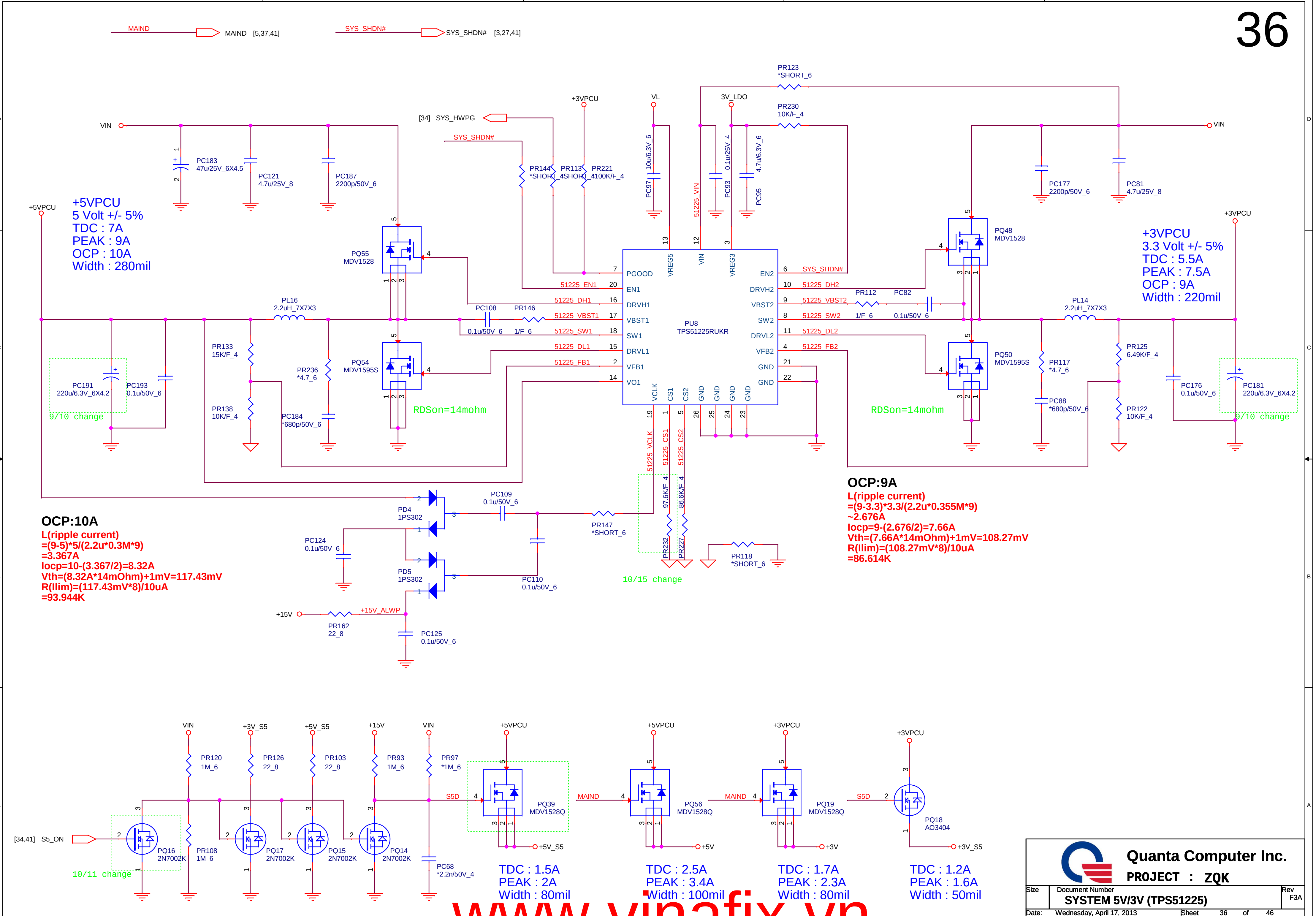

MAIND [5,37,41]
SYS_SHDN# [3,27,41]
+5VPCU
5 Volt +/- 5%
TDC : 7A
PEAK : 9A
OCP : 10A
Width : 280mil
+3VPCU
3.3 Volt +/- 5%
TDC : 5.5A
PEAK : 7.5A
OCP : 9A
Width : 220mil
PU8
TPS51225RUKR
PGOOD
EN1
DRVH1
VBST1
SW1
DRVL1
VFB1
VO1
EN2
DRVH2
VBST2
SW2
DRVL2
VFB2
GND
VREG5
VIN
VREG3
VCLK
CS1
CS2
[34] SYS_HWPG
PQ55
MDV1528
PQ54
MDV1595S
PQ48
MDV1528
PQ50
MDV1595S
PL16
2.2uH_7X7X3
PL14
2.2uH_7X7X3
PC183
47u/25V_6X4.5
PC121
4.7u/25V_8
PC187
2200p/50V_6
PC177
2200p/50V_6
PC81
4.7u/25V_8
PC97
10u/6.3V_6
PC93
0.1u/25V_4
PC95
4.7u/6.3V_6
PR123
*SHORT_6
PR230
10K/F_4
PR144
*SHORT_4
PR113
*SHORT_4
PR221
100K/F_4
PC108
0.1u/50V_6
PR146
1/F_6
PR112
1/F_6
PC82
0.1u/50V_6
PR133
15K/F_4
PR138
10K/F_4
PR236
*4.7_6
PC184
*680p/50V_6
PR117
*4.7_6
PC88
*680p/50V_6
PR125
6.49K/F_4
PR122
10K/F_4
PC191
220u/6.3V_6X4.2
PC193
0.1u/50V_6
PC176
0.1u/50V_6
PC181
220u/6.3V_6X4.2
9/10 change
RDSon=14mohm
PD4
1PS302
PD5
1PS302
PC109
0.1u/50V_6
PC110
0.1u/50V_6
PC124
0.1u/50V_6
PR147
*SHORT_6
PR232
97.6K/F_4
PR227
86.6K/F_4
PR118
*SHORT_6
10/15 change
+15V
PR162
22_8
+15V_ALWP
PC125
0.1u/50V_6
OCP:10A
L(ripple current)
=(9-5)*5/(2.2u*0.3M*9)
=3.367A
Iocp=10-(3.367/2)=8.32A
Vth=(8.32A*14mOhm)+1mV=117.43mV
R(Ilim)=(117.43mV*8)/10uA
=93.944K
OCP:9A
L(ripple current)
=(9-3.3)*3.3/(2.2u*0.355M*9)
~2.676A
Iocp=9-(2.676/2)=7.66A
Vth=(7.66A*14mOhm)+1mV=108.27mV
R(Ilim)=(108.27mV*8)/10uA
=86.614K
[34,41] S5_ON
PQ16
2N7002K
PR120
1M_6
PR108
1M_6
PR126
22_8
PQ17
2N7002K
PR103
22_8
PQ15
2N7002K
PR93
1M_6
PQ14
2N7002K
PR97
*1M_6
PC68
*2.2n/50V_4
10/11 change
PQ39
MDV1528Q
+5V_S5
TDC : 1.5A
PEAK : 2A
Width : 80mil
PQ56
MDV1528Q
+5V
TDC : 2.5A
PEAK : 3.4A
Width : 100mil
PQ19
MDV1528Q
+3V
TDC : 1.7A
PEAK : 2.3A
Width : 80mil
PQ18
AO3404
+3V_S5
TDC : 1.2A
PEAK : 1.6A
Width : 50mil
Quanta Computer Inc.
PROJECT : ZQK
Size
Document Number
SYSTEM 5V/3V (TPS51225)
Rev
F3A
Date: Wednesday, April 17, 2013
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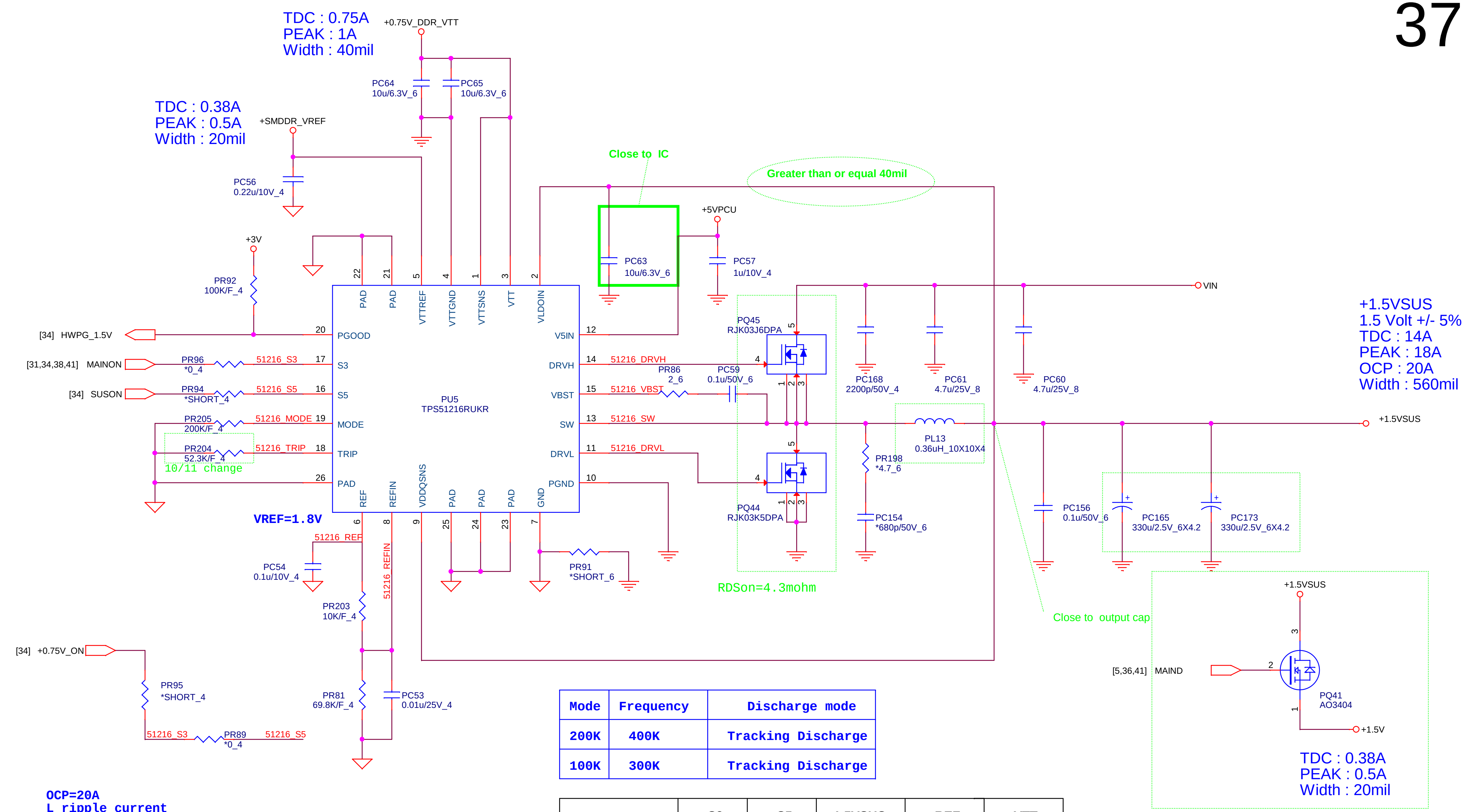


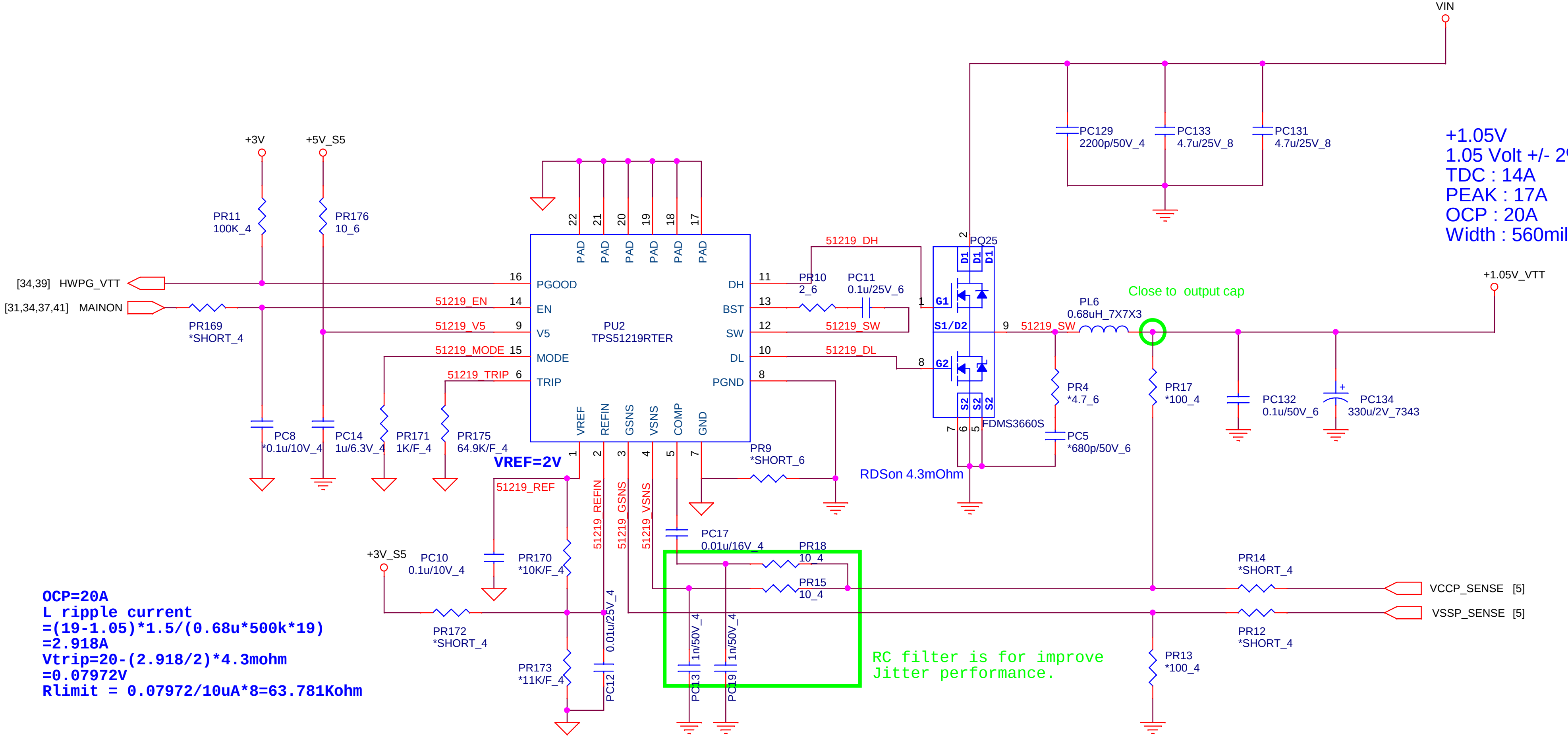
Mode	Frequency	Discharge mode
200K	400K	Tracking Discharge
100K	300K	Tracking Discharge

OCP=20A
L ripple current
=(19-1.5)*1.5/(0.36u*400k*19)
=9.594A
Vtrip=20-(9.594/2)*4.3mohm
=0.065372V
Rlimit=0.065372/10uA*8=52.297Kohm

	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

Quanta Computer Inc.
PROJECT : ZQK

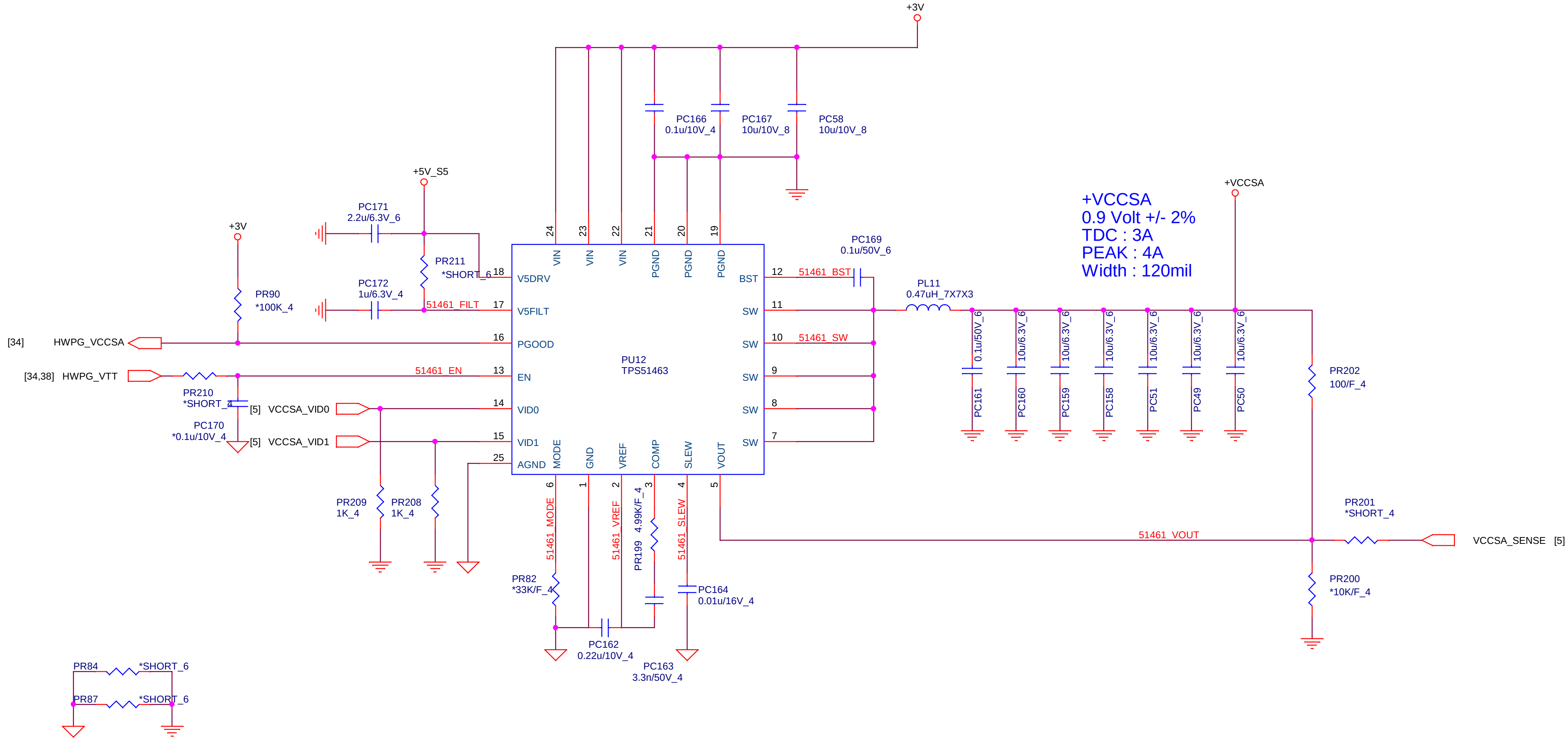
Size | Document Number: DDR 1.5V(TPS51216) | Rev F3A
Date: Wednesday, April 17, 2013 | Sheet 37 of 46



+1.05V
1.05 Volt +/- 2%
TDC : 14A
PEAK : 17A
OCP : 20A
Width : 560mil

OCP=20A
L ripple current
=(19-1.05)*1.5/(0.68u*500k*19)
=2.918A
Vtrip=20-(2.918/2)*4.3mohm
=0.07972V
Rlimit = 0.07972/10uA*8=63.781Kohm

Quanta Computer Inc.	PROJECT : ZQK
Size	Document Number: +1.05V (TPS51219) — Rev F3A
Date: Wednesday, April 17, 2013	Sheet 38 of 46



VID0	VID1	+VCCSA
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

default 0.9V

Quanta Computer Inc.

PROJECT : ZQK

Size | Document Number: VCCSA(TPS51463) | Rev: F3A

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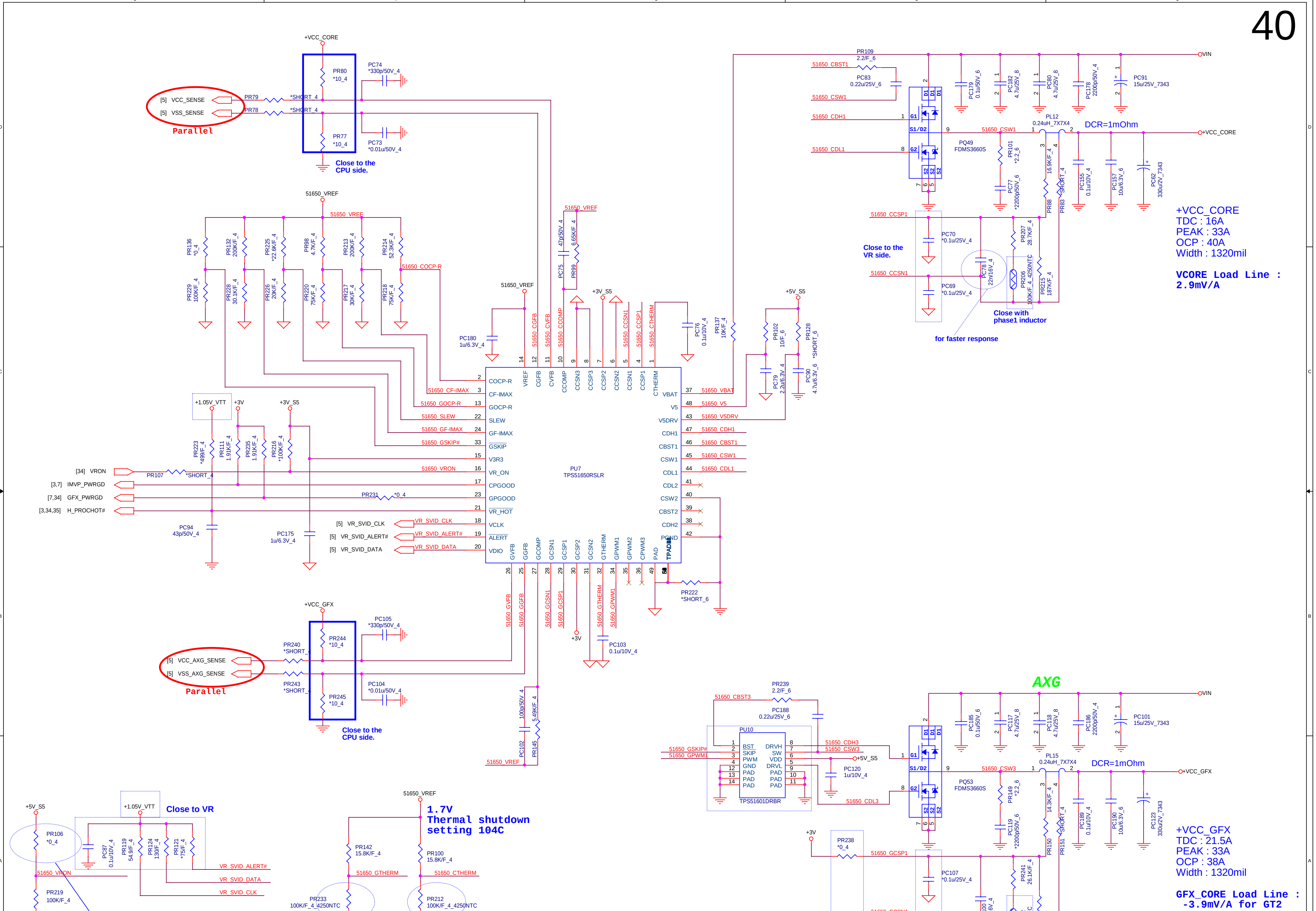

Quanta Computer Inc.

PROJECT : ZQK

Size | Document Number: +VCC_CORE/+VGFX (TPS51650) | Rev F3A

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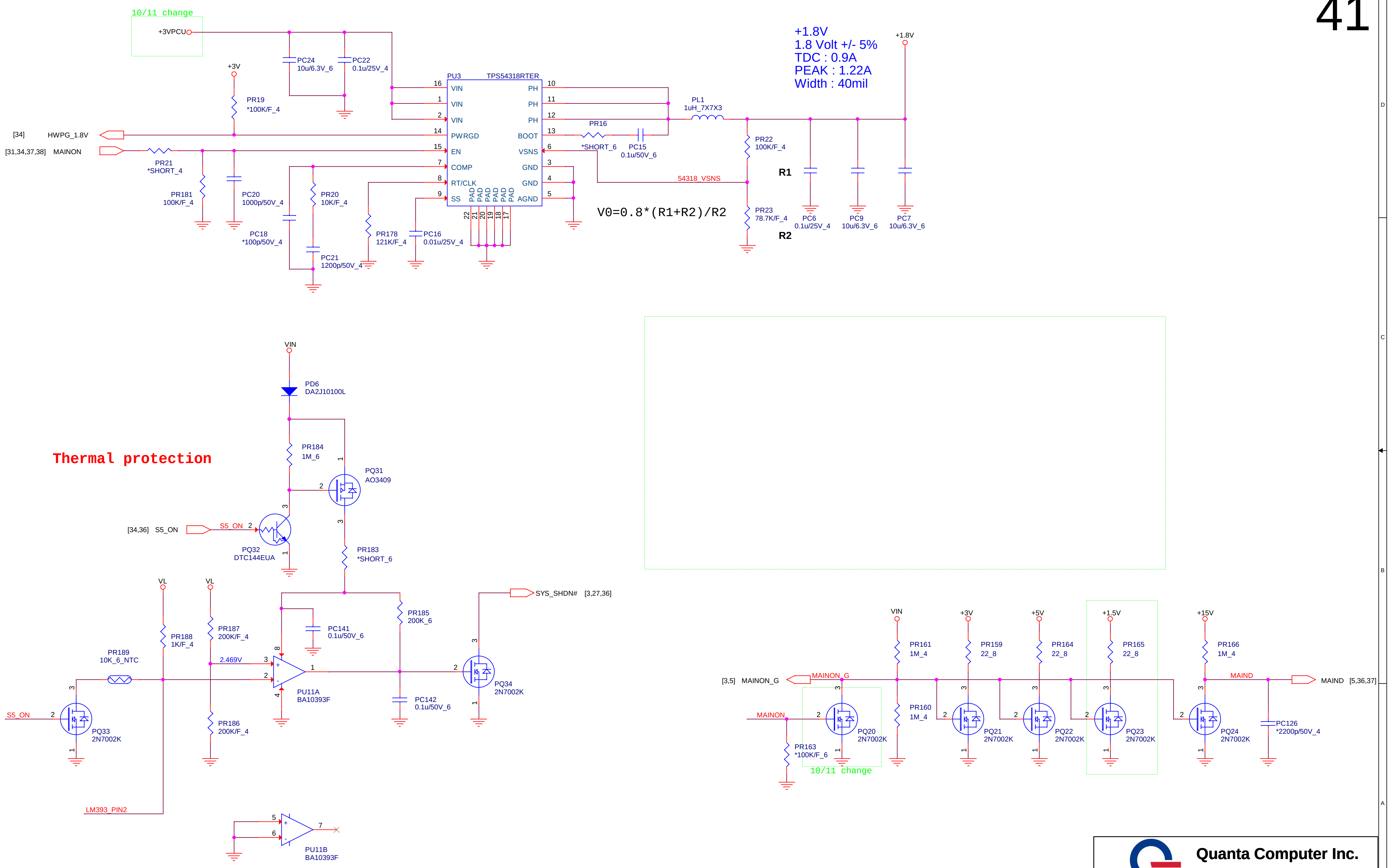
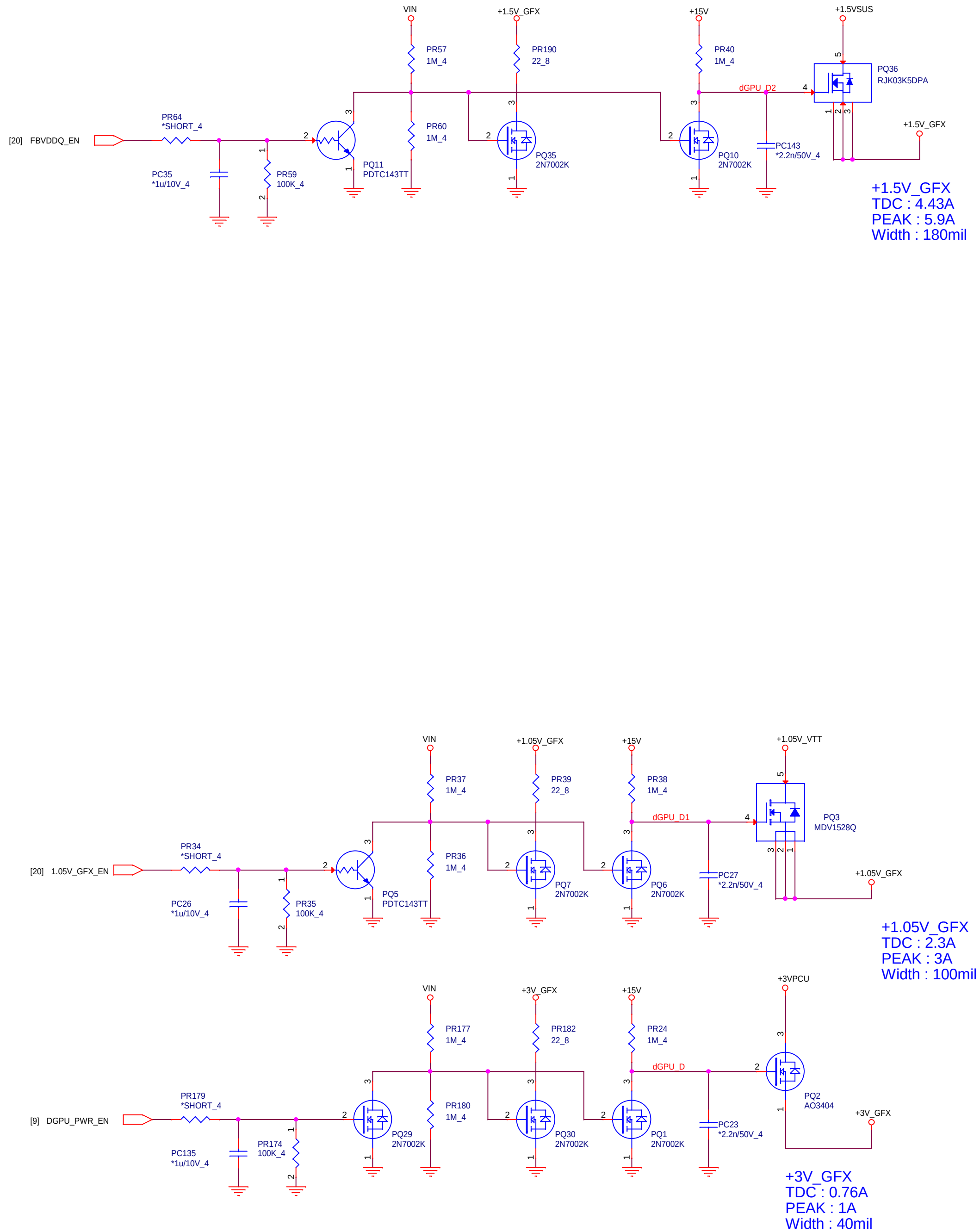


For EC control thermal protection (output 3.3V)

Quanta Computer Inc.

PROJECT : ZQK

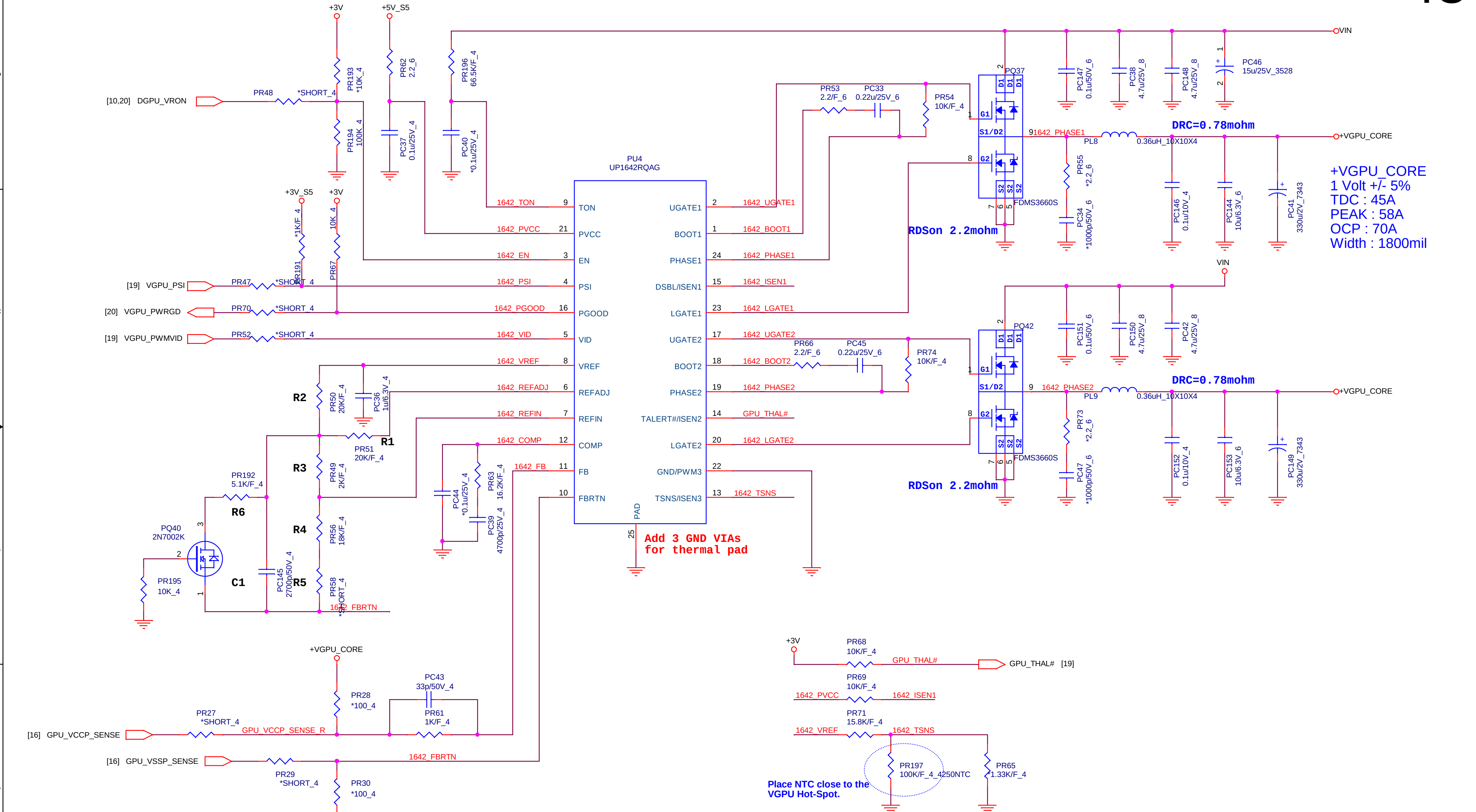
Size	Document Number	Rev
	+1.8V/Discharge/Thermal	F3A
Date: Wednesday, April 17, 2013	Sheet 41 of 43	



Quanta Computer Inc.

PROJECT : ZQK

Size	Document Number	Rev
	+VGPU_CORE(UP1642PQAG)	F3A
Date: Wednesday, April 17, 2013	Sheet 42 of 46	



Quanta Computer Inc.

PROJECT : ZQK

Size	Document Number	Rev
	+VGPU_CORE(UP1642PQAG)	F3A
Date: Wednesday, April 17, 2013	Sheet 43 of 46	